FINAL REPORT

for

PLATED WIRE MEMORY SUBSYSTEM

October 1972 - February 1974

Contract No.: NAS5-23163

Prepared by

Motorola Inc.

Government Electronics Div.

Scottsdale, Arizona

for

Goddard Space Flight Center

Greenbelt, Maryland

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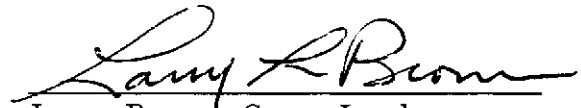

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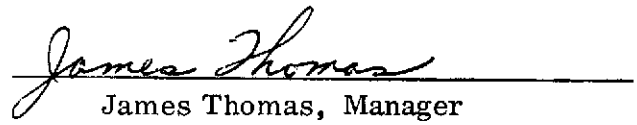

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Aerospace Data Section

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SECTION 1

INTRODUCTION AND OVERALL PROGRAM SUMMARY

1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola, Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS5-23163. The report is submitted in accordance with the requirements of Specifications S-562-P-24 (Rev. 2) and covers the period from October 1972 to February 1974.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the construction and testing of a 4096 word by 18 bit random access, NDRO Plated Wire Memory for use in conjunction with a Spacecraft Input/Output Unit and Central Processing Unit.

The primary design parameters, in order of importance, were high reliability, low power, volume and weight. Two memory units, Serial No. 101 and 102, were delivered.

1.2 RESULTS ATTAINED

The memory units were subjected to comprehensive functional and environmental testing at the end-item level to verify conformance with the specified requirements. Contract modifications were necessary in some areas, either to relax the requirements or to redefine noncritical parameters. All such modifications were relatively insignificant, with the possible exception of system weight and operating power consumption.

A comparison of the memory units most significant physical and performance characteristics versus the specified requirements is shown in Table I.

Table I. Memory Performance Vs. Specified Requirements

Characteristic	Contract Reference	Specified	Measured
Volume	S-562-P-24 (Rev. 2)	160 in^3	159.45 in^3
Weight	S-562-P-24 (Rev. 2) Mod. 3 (7-24-73)	6 lbs 6.5 lbs	6.25 lbs.
Power (Operate)	S-562-P-24 (Rev. 2) Mod. 3 (7-24-73)	6 watts 7 watts	6.68 watts (102) 6.29 watts (101)
Power (Standby)	S-562-P-24 (Rev. 2)	170 milliwatts	130.8 mW (102) 127.6 mW (101)
Voltage Tolerance	S-562-P-24 (Rev. 2)	±5% on all	±5% on all
Operating Rate	S-562-P-24 (Rev. 2) Mod. 2 (3-16-73)	500 kHz 600 kHz	 >600 kHz
Access Time	S-562-P-24 (Rev. 2)	500 nanoseconds	<500 nanoseconds
Operating Temp.	S-562-P-24 (Rev. 2)	-40°C to +85°C	Tested from -40°C to +85°C
Operating Vacuum	S-562-P-24 (Rev. 2) Mod. 3 (7-24-73)	One Atm. to 10^{-6} mm Hg. One Atm. to 10^{-5} mm Hg. (Modified for test purposes)	 Tested from one Atm. to 10^{-5} mm Hg.
Operating Vibration	S-562-P-24 (Rev. 2)	Sinusoidal: 5-25 Hz, 0.5 in DA 25-110 Hz, 15 g Peak 110-2000 Hz, 7.5g Peak Two Octaves/ Minute Random: 15 Hz, 0.01g^2/ Hz 15-70 Hz, Linear In-crease 70-100 Hz,	

Table I. Memory Performance vs. Specified Requirements (Contd)

Characteristic	Contract Reference	Specified	Measured
Operating Vibration (Contd)		0.31g^2/Hz 100-400 Hz. Linear Decrease 400-2000 Hz, 0.02g^2/Hz Two Min./ Axis	
	Mod. 4(7-24-73)	Sinusoidal: 5-25 Hz, 0.33 in DA 25-110 Hz, 10g Peak 110-2000 Hz, 5g Peak Two Octaves/ Minute Random: 15 Hz, .0004g^2/Hz 15-70 Hz, Linear Increase 70-100 Hz, .138g^2/Hz 100-400 Hz, Linear Decrease 400-2000 Hz, .0089g^2/Hz	Tested at Mod. 4 levels
Operating Shock	S-562-P-24 (Rev. 2)	Two Shock Pulses of 30g for 6 and 12 milliseconds in three directions.	Tested at specified levels.

SECTION 2

HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design, construction and test history, as related to the hardware requirements of this contract, is summarized in this section. The summarization is in chronological order from date of contract award to date of final delivery of the memory units. Design activity began on both units on 5 October 1972.

2.1 SERIAL NUMBER 101

Assembly was completed and testing began in April 1973. An analysis of the test results indicated that design problems were limited to the performance of the memory at voltage and temperature extremes. The unit worked over much of the design range and it was jointly decided (GSFC TWX 4 June 1973) to deliver the unit to GSFC for temporary use while the problems were analyzed and corrected in S/N 102. The unit was shipped to GSFC in June after temperature tests only. After GSFC received S/N 102, S/N 101 was returned to Motorola in August 1973 for modification and test. S/N 101 was modified with all design changes made as a result of S/N 102 testing. The unit was acceptance tested and shipped to GSFC on 7 November 1973.

The memory was again returned to Motorola on January 16, 1974 . To be modified to correct the very low repetition rate problem discovered in S/N 102. Modification to correct the problem was completed, and the memory was tested and shipped on February 15, 1974.

2.2 SERIAL NUMBER 102

Assembly was completed and testing began in May 1973. During the Y-axis sine vibration test, on 6/21/73, bit errors were noted at 20 Hz, 130 Hz and 408 Hz. The unit was removed from the housing and inspected, thereby revealing broken pins on the word drive interconnect. Analysis indicated that the interconnect was too rigid to allow for deflection at the center of the electronics and plane boards.

Rigidity in the horizontal direction was reduced by cutting the printed circuit board and completing the connections with stranded, teflon insulated wire. Relative motion between the horizontal connectors is accommodated through the flexible wiring. (See Figure 2.) The unit was then retested at 8.4 G rms with no problems.

As a result of the design analysis and testing results, several design changes and performance modifications were requested and approved by GSFC (TWX dated 26 July 1973). These included the addition of Mu-metal shielding, change of interconnect board design as described, decrease of negative supply voltage from -6.9 Vdc to -6.1 Vdc, increase in allowable operating power to 7 watts and allowable weight to 6.5 pounds, and reduction of vacuum specification from 10^{-6} mmHg to 10^{-5} mmHg.

S/N 102 passed the acceptance tests and was shipped on 7/30/73.

At GSFC it was discovered that S/N 102 exhibited repeatable bit errors when operated with a low repetition rate initiate pulse. The unit was returned to Motorola on 8/21/73 where the problem was verified. It was determined that during final checkout this problem was not adequately tested. Checkout procedures were modified to fully exercise the memory.

Several design changes were made to correct the low repetition rate problem and provide more consistent memory operation. These changes included word selection circuitry bias and restore timing changes, addition of power supply decoupling capacitors on the digit drivers, and grounding methods in the memory stack. On 10/15/73, S/N 102 completed an abbreviated AT (per GSFC TWX dated 9/14/73) and was shipped to GSFC.

GSFC discovered a very low repetition rate problem (about 0.3 Hz) and returned the memory to Motorola on December 4, 1973. Analysis indicated that the voltage at the collectors of the Level 1 select transistors when both the Level 1 and Level 2 select transistors had been off for several hundred milliseconds, tended to rise to the +5 volt supply voltage due to leakage currents through the reversed biased base-emitter junctions of the Level 2 select transistors (see Figure 13).

Upon selection of particular Level 1 and Level 2 select transistor, the base-emitter capacitance couples a negative voltage pulse onto the Level 2 select lines. This negative pulse turns on unwanted Level 2 select transistors, robbing current from the addressed word line and allowing current to flow down unselected word lines. This causes a net differential signal at the sense amplifier inputs which can be of the wrong polarity, resulting in an error.

The problem was solved by providing a leakage path to ground from the Level 1 collector point to prevent that point from rising above ground potential. This was accomplished by adding sixty-four 10k ohm, 1/8 watt, carbon composition resistors; four on each side of each of eight memory planes; three by lap soldering one end of each resistor to a word select flat pack pin or PC board track and the other end of each resistor to a plated - through hole in the memory plane ground layer; one by soldering one end as above and lap soldering the other end to a ground pad. (See Memory Plane Assembly 01-P13720D included as an insert at the back of this report.) All resistors were bonded to the PC board. A modified acceptance test was performed and the memory was returned to GSFC on January 18, 1974.

SECTION 3

TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figures 1 and 2. They are identified as Motorola Part Number 01-P13701D001. Serial Numbers 101 and 102.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Numbers 01-P13701D, 15-P13703D, and 15-13702D (included in the engineering drawing package submitted to GSFC) completely define the end-item package in terms of size, mounting pattern, finish, etc. Drawing 69-P13705D, Interconnection Diagram, is included as an insert at the back of this report. The weight of the delivered unit was 6.25 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 3 Memory System Electrical Interface).

1. 18 Input Data Lines (to memory)
2. 16 Input Address Lines (to memory)
3. 18 Output Data Lines (from memory)
4. 1 Initiate Line (to memory)
5. 1 Read/Write Select Line (to memory)
6. 1 Read Complete Line (from memory)
7. 2 Thermistor Sensor Lines (from memory)
8. 7 Lines for -6.1V (to memory - all lines common internally)
9. 5 Lines for +5.0V (to memory - all lines common internally)
10. 12 Lines for Power and Signal Return (all lines common internally)

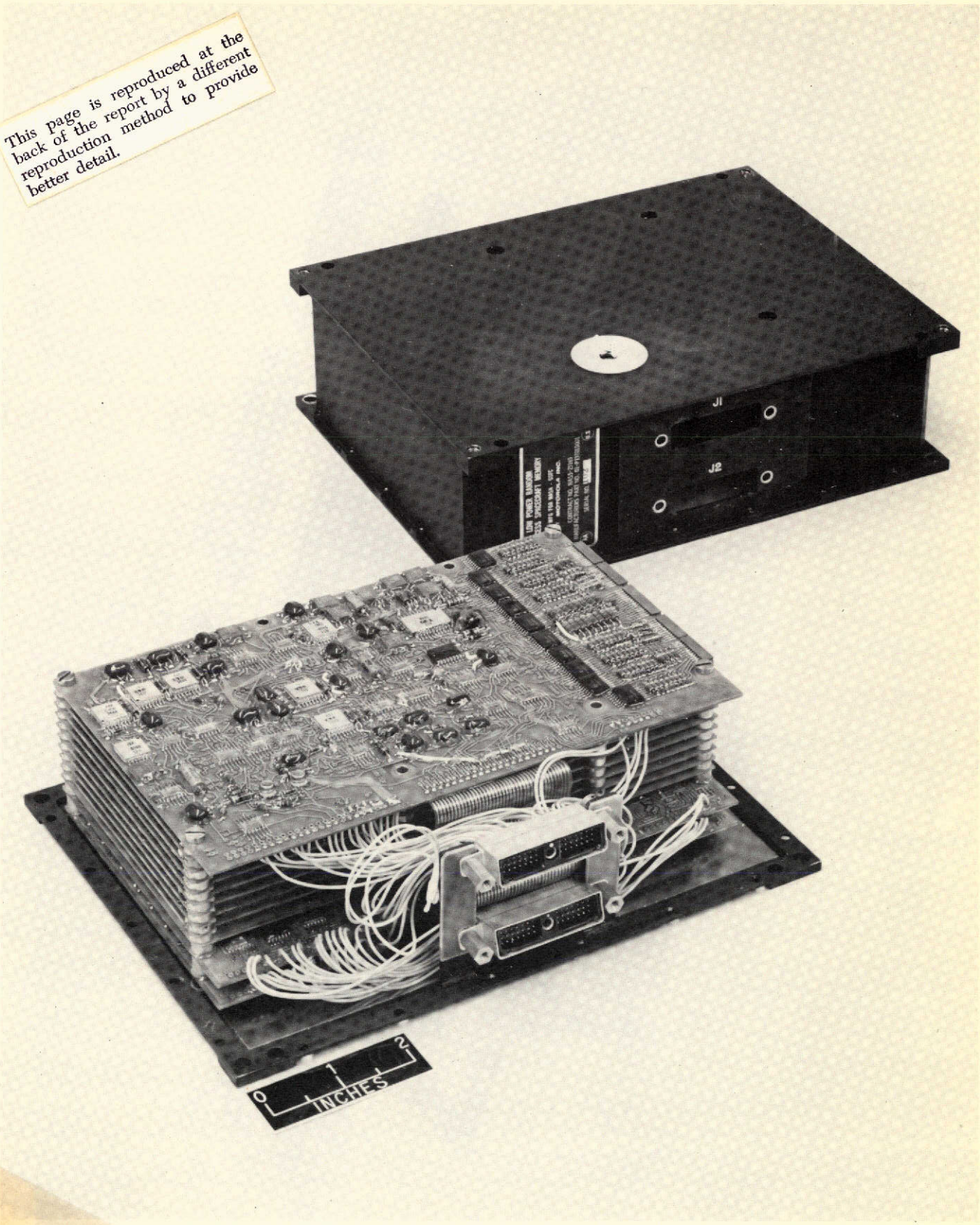

Figure 1. 4K x 18 Bit Plated Wire Memory System

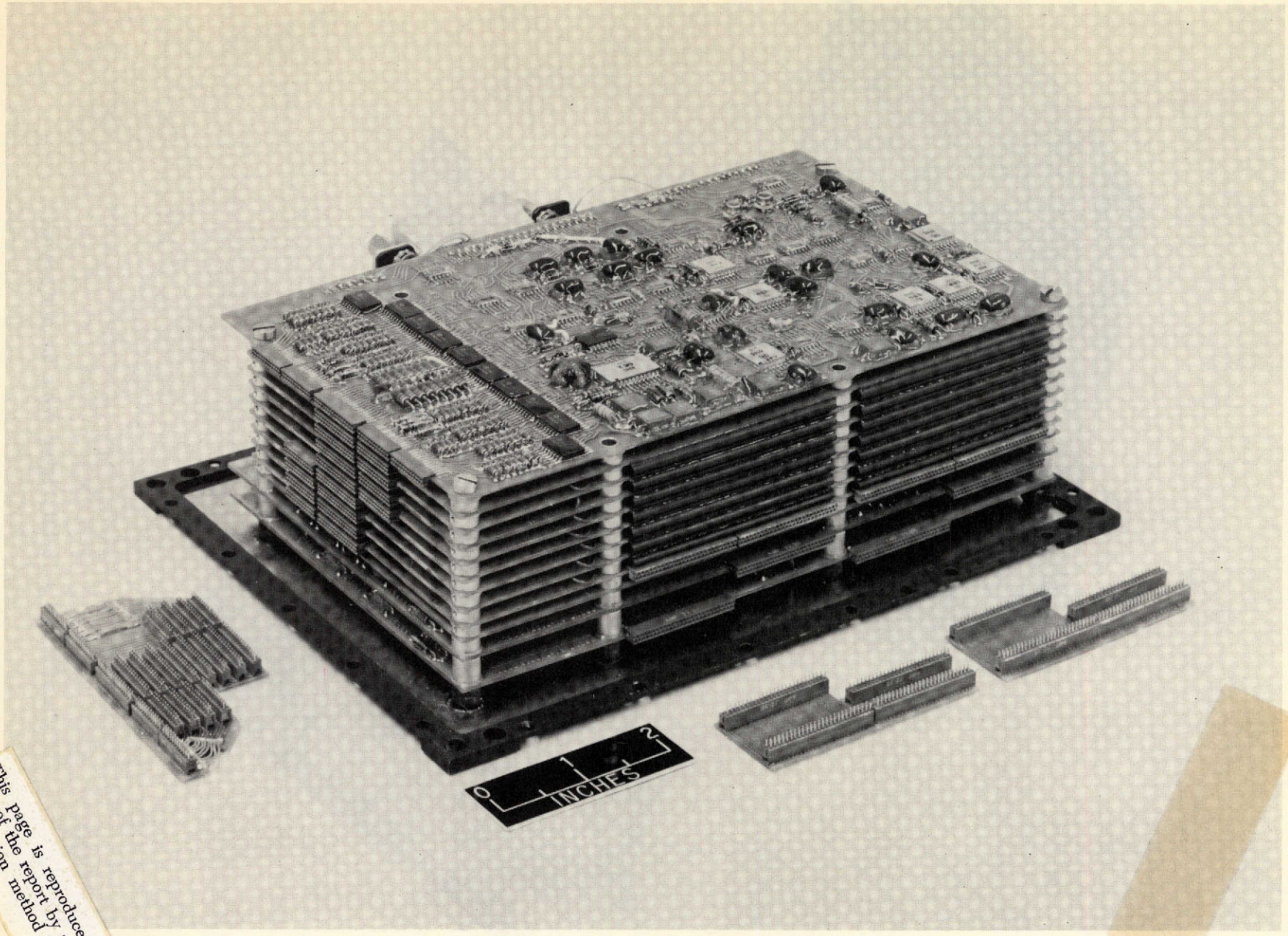

Figure 2. 4K x 18 Bit Plated Wire Memory System Stack

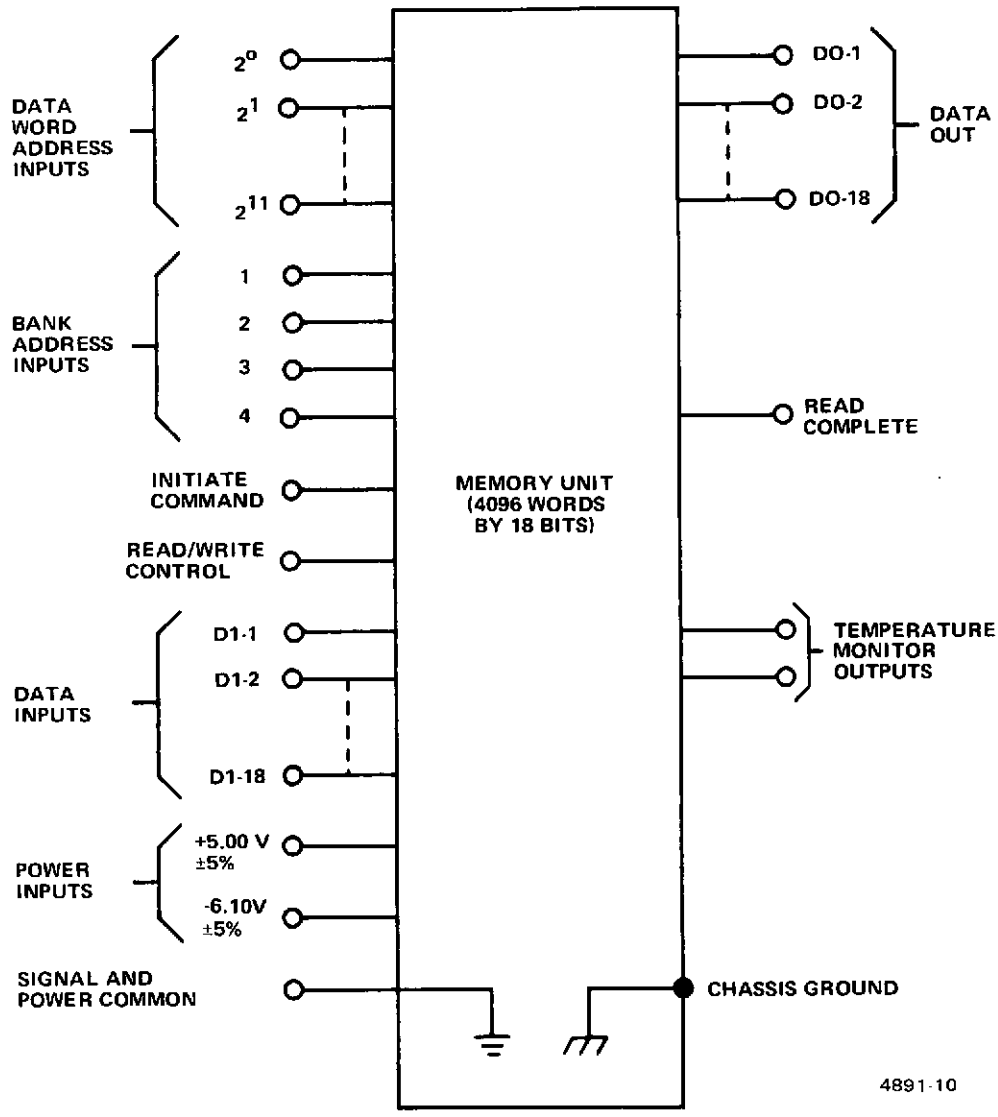

Figure 3. Memory System Electrical Interface

The connector pin designations are as given in Table II.

All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

Memory Capacity: 4096 words of 18 bits each (73,728 bits total).

Access: Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

Access Time: 350 nanoseconds, maximum, from leading edge of Initiate signal.

Read Cycle Time: 1.20 microseconds, maximum, from leading edge of Initiate signal.

Write Cycle Time: 1.00 microseconds, maximum, from leading edge of Initiate signal.

Operate Rate: 0 to 600k operations per second, minimum, with any read/write ratio.

Initiate Signal: Active level = logic ONE. Minimum pulse width = 50 nanoseconds. Maximum pulse width = 550 nanoseconds.

Read/Write Select: Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

Bank Address Lines: Must be stable from leading edge of Initiate pulse to end of Read or Write cycle.

Word Address Lines: Must be stable from leading edge of Initiate to end of cycle time.

Table II. External Connector Pin Assignments

Pin No.	Function	Pin No.	Function
J1-1A	Address Bit 2^0	J2-1A	Data Input Bit 2^0
-1B	Address Bit 2^1	-1B	Data Input Bit 2^1
-1C	Address Bit 2^2	-1C	Data Input Bit 2^2
-1D	Address Bit 2^3	-1D	Data Input Bit 2^3
-1E	Address Bit 2^4	-1E	Data Input Bit 2^4
-1F	Address Bit 2^5	-1F	Data Input Bit 2^5
-1G	Address Bit 2^6	-1G	Data Input Bit 2^6
-1H	Return	-1H	Data Input Bit 2^7
-1J	Read/Write Control	-1J	Data Input Bit 2^8
-1K	Return	-1K	Data Input Bit 2^9
-1L	Return	-1L	Data Input Bit 2^{10}
-1M	Return	-1M	Data Input Bit 2^{11}
-1N	Initiate Command	-1N	Data Input Bit 2^{12}
-1P	Not Assigned	-1P	Data Input Bit 2^{13}
-2A	Address Bit 2^7	-2A	Data Input Bit 2^{14}
-2B	Address Bit 2^8	-2B	Data Input Bit 2^{15}
-2C	Address Bit 2^9	-2C	Data Input Bit 2^{16}
-2D	Address Bit 2^{10}	-2D	Data Input Bit 2^{17}
-2E	Address Bit 2^{11}	-2E	Data Output Bit 2^0
-2F	Bank Address Bit 0	-2F	Data Output Bit 2^1
-2G	Bank Address Bit 1	-2G	Data Output Bit 2^2
-2H	-6.1V	-2H	Data Output Bit 2^3
-2J	-6.1V	-2J	Data Output Bit 2^4
-2K	-6.1V	-2K	Data Output Bit 2^5
-2L	-6.1V	-2L	Data Output Bit 2^6
-2M	-6.1V	-2M	Data Output Bit 2^7
-2N	-6.1V	-2N	Data Output Bit 2^8

Table II. External Connector Pin Assignments (Contd)

Pin No.	Function	Pin No.	Function
J1-2P	-6.1V	J2-2P	Data Output Bit 2^9
-3A	Bank Address Bit 2	-3A	Data Output Bit 2^{10}
-3B	Bank Address Bit 3	-3B	Data Output Bit 2^{11}
-3C	+5.0V	-3C	Data Output Bit 2^{12}
-3D	+5.0V	-3D	Data Output Bit 2^{13}
-3E	+5.0V	-3E	Data Output Bit 2^{14}
-3F	+5.0V	-3F	Data Output Bit 2^{15}
-3G	+5.0V	-3G	Data Output Bit 2^{16}
-3H	Thermistor	-3H	Data Output Bit 2^{17}
-3J	Thermistor	-3J	Return
-3K	Read Complete	-3K	Return
-3L	Return	-3L	Return
-3M	Return	-3M	Return
-3N	Not Assigned	-3N	Return
-3P	Not Assigned	-3P	Return

Input Date Lines: For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

Read Complete Line: Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 350 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

Data Output Lines: Presents high impedance state (20k minimum) in quiescent state. Goes active (i.e. low impedance) maximum of 30 nanoseconds following leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. Will sink minimum of 10 mA at 0.3 V in active state.

3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.1V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

+5.0V:

Regulation: ±5%

Average Standby Current: 13.1 mA, worst-case.

Average Operate Current: 840 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 50 mA, maximum, during cycle time.

Standby Power: 68.8 milliwatts maximum at +5.25V.

Operate Power: 4.41 watts, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

-6.1V:

Regulation: ±5%

Average Standby Current: 10.9 mA, worst-case.

Average Operate Current: 355 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 60 mA, maximum, during cycle time.

Standby Power: 69.8 milliwatts, maximum, at -6.40 volts.

Operate Power: 2.27 watts, maximum, at -6.40 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table III.

Table III. Thermistor Resistance Versus Temperature

RESISTANCE VERSUS TEMPERATURE -80°C to +150°C																							
TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES
−80	3558K	−50	441.3K	−20	78.91K	+10	18.79K	+40	5592	+70	1990	+100	816.8	+130	376.4
79	3296K	49	414.5K	19	74.91K	11	17.98K	41	5389	71	1928	101	794.6	131	367.4
78	3055K	48	389.4K	18	71.13K	12	17.22K	42	5193	72	1868	102	773.1	132	358.7
77	2833K	47	366.0K	17	67.57K	13	16.49K	43	5006	73	1810	103	752.3	133	350.3
76	2629K	46	344.1K	16	64.20K	14	15.79K	44	4827	74	1754	104	732.1	134	342.0
75	2440K	45	323.7K	15	61.02K	15	15.13K	45	4655	75	1700	105	712.6	135	334.0
74	2266K	44	304.6K	14	58.01K	16	14.50K	46	4489	76	1648	106	693.6	136	326.3
73	2106K	43	286.7K	13	55.17K	17	13.90K	47	4331	77	1598	107	675.3	137	318.7
72	1957K	42	270.0K	12	52.48K	18	13.33K	48	4179	78	1549	108	657.5	138	311.3
71	1821K	41	254.4K	11	49.94K	19	12.79K	49	4033	79	1503	109	640.3	139	304.2
−70	1694K	−40	239.8K	−10	47.54K	+20	12.26K	+50	3893	+80	1458	+110	623.5	+140	297.2
69	1577K	39	226.0K	9	45.27K	21	11.77K	51	3758	81	1414	111	607.3	141	290.4
68	1469K	38	213.2K	8	43.11K	22	11.29K	52	3629	82	1372	112	591.6	142	283.8
67	1369K	37	201.1K	7	41.07K	23	10.84K	53	3504	83	1332	113	576.4	143	277.4
66	1276K	36	189.8K	6	39.14K	24	10.41K	54	3385	84	1293	114	561.6	144	271.2
65	1190K	35	179.2K	5	37.31K	25	10.00K	55	3270	85	1255	115	547.3	145	265.1
64	1111K	34	169.3K	4	35.57K	26	9605	56	3160	86	1218	116	533.4	146	259.2
63	1037K	33	160.0K	3	33.93K	27	9227	57	3054	87	1183	117	519.9	147	253.4
62	968.4K	32	151.2K	2	32.37K	28	8867	58	2952	88	1149	118	506.8	148	247.8
61	904.9K	31	143.0K	− 1	30.89K	29	8523	59	2854	89	1116	119	494.1	149	242.3
−60	845.9K	−30	135.2K	0	29.49K	+30	8194	+60	2760	+90	1084	+120	481.8	+150	237.0
59	791.1K	29	127.9K	+ 1	28.15K	31	7880	61	2669	91	1053	121	469.8		
58	740.2K	28	121.1K	2	26.89K	32	7579	62	2582	92	1023	122	458.2		
57	692.8K	27	114.6K	3	25.69K	33	7291	63	2497	93	994.2	123	446.9		
56	648.8K	26	108.6K	4	24.55K	34	7016	64	2417	94	966.3	124	435.9		
55	607.8K	25	102.9K	5	23.46K	35	6752	65	2339	95	939.3	125	425.3		
54	569.6K	24	97.49K	6	22.43K	36	6500	66	2264	96	913.2	126	414.9		
53	534.1K	23	92.43K	7	21.45K	37	6258	67	2191	97	887.9	127	404.9		
52	501.0K	22	87.66K	8	20.52K	38	6026	68	2122	98	863.4	128	395.1		
51	470.1K	21	83.16K	9	19.63K	+39	5805	69	2055	99	839.7	129	385.6		

RR-6

3.3 FUNCTIONAL DESCRIPTION

3.3.1 Memory Organization

The memory is organized into 1024 memory words of 72 bits each (expandable to 96 bits). Each memory word therefore comprises four 18-bit external data words. Figure 4 is a block diagram of the memory organization. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

Using two wires for each bit storage (i.e., two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

The only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics is packaged on three similar board assemblies.

3.3.2 Word-Line Selection and Drive

Figures 5 and 6 show the word current selection and drive method. Word line addressing is accomplished through a two-level tree of transistor switches. The first level steers the word current to one of 64 unique areas of the stack. The second level steers the word current into one of 16 word lines in the particular word group addressed through the first level. Both levels are packaged on the memory stack boards.

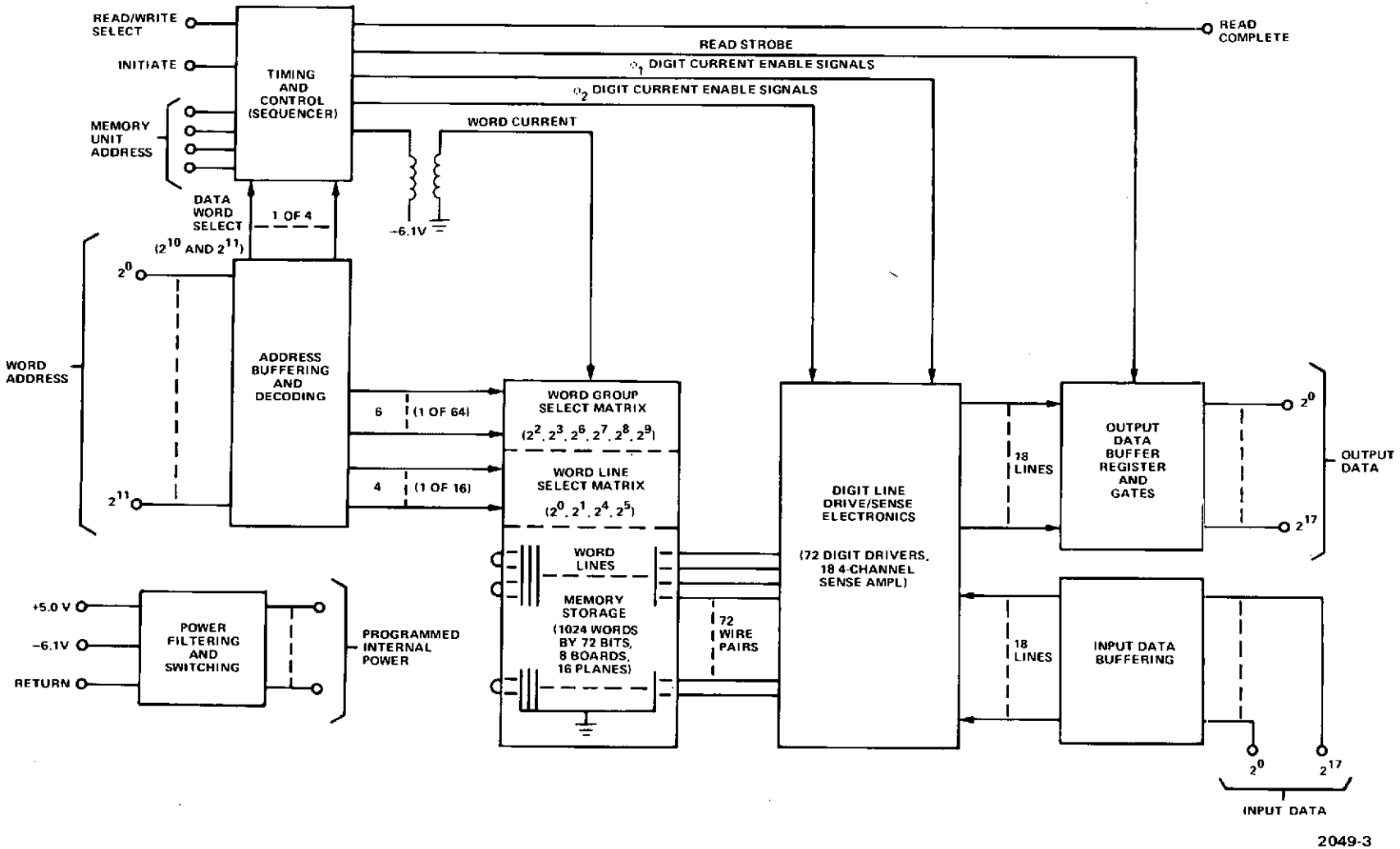

Figure 4. Overall Functional Block Diagram

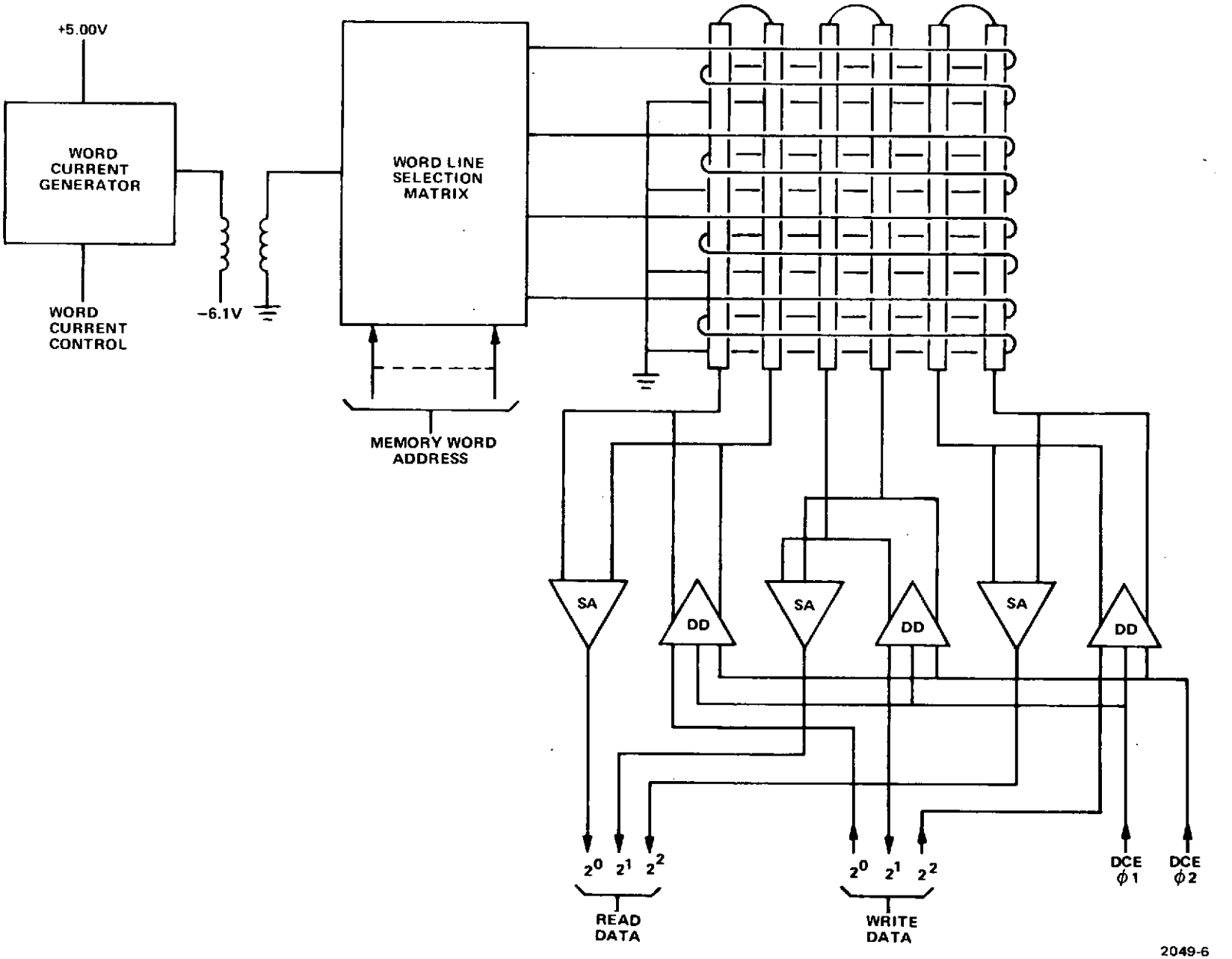

Figure 5. Simplified Memory Drive and Sense Diagram

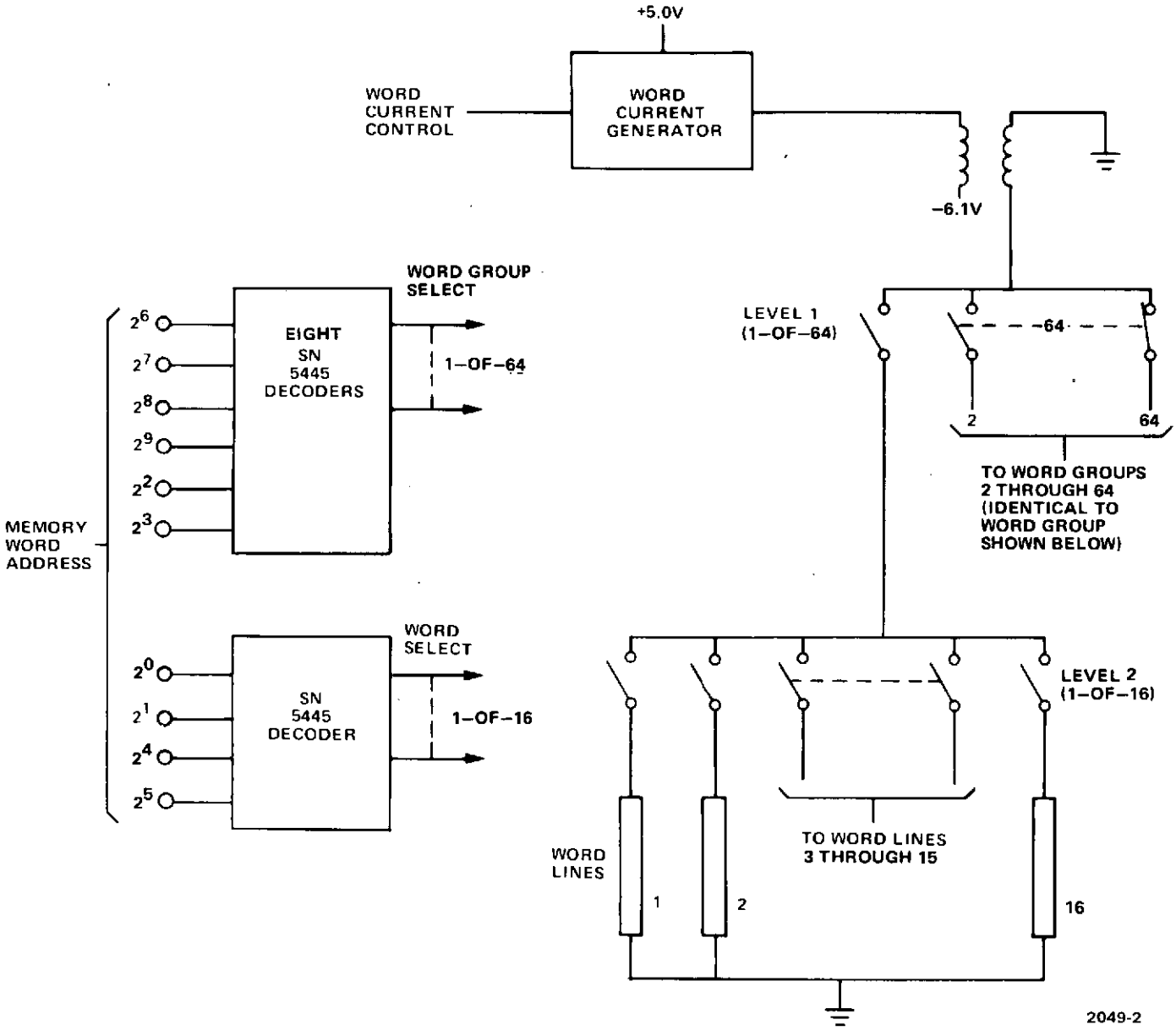

Figure 6. Word-Line Selection Matrix

The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits 2^2, 2^3 and 2^6 through 2^9 are decoded into 1-of-64 and identify the word group. Bits 2^0, 2^1, 2^4 and 2^5 are decoded into 1-of-16 and identify the word line within a group. Bits 2^{10} and 2^{11} identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight binary code.

Since only one end of each word line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing

The memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 7. Each delay is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay τ_A (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers and associated logic is also controlled through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays τ_B through τ_E are activated for a write cycle. Delays τ_B and τ_D set the width of the two phases of digit current and τ_C sets the separation between the two phases. Delay τ_E controls the duration of the word current. The ϕ_1 and ϕ_2 digit current controls for one of the four possible data words are activated, depending on the states of address bits 2^{10} and 2^{11}.

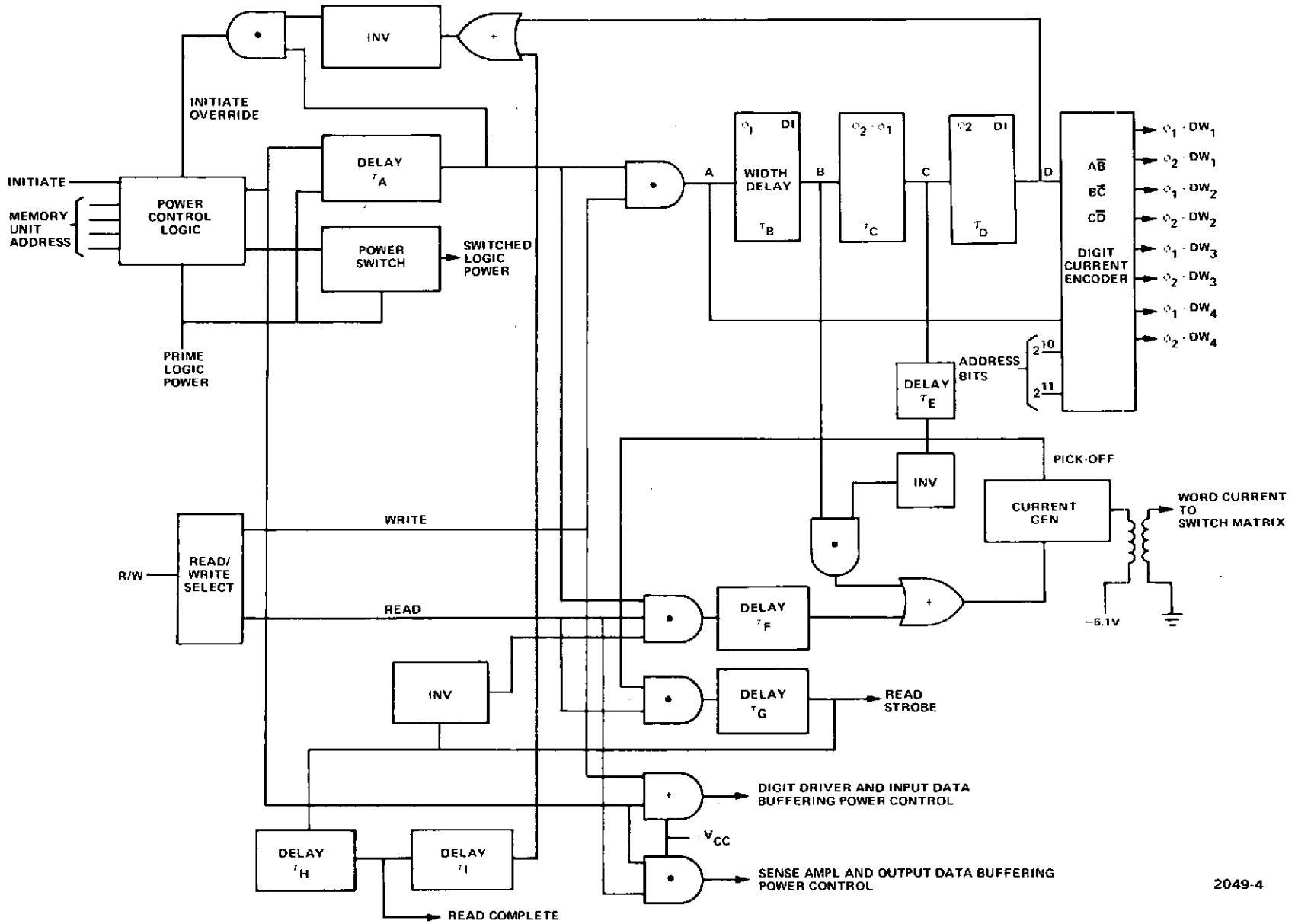

Figure 7. Sequencer, Logic Diagram

Delays τ_F through τ_I are activated during a read cycle. Delay τ_F starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by τ_G and used as the read strobe, which clocks the sense amplifier outputs into the output data buffer register. Delays τ_H and τ_I set the duration of the read complete and the post-read data hold periods, respectively.

3.3.4 Write Operation

The memory timing for a write cycle is shown in **Figure 8.** For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits 2^0 through 2^9. A group of 18 digit driver current sources is then energized for ϕ_1 current. The particular current sources are identified by address bits 2^{10} and 2^{11}. The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The ϕ_1 digit current is then terminated and ϕ_2 current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

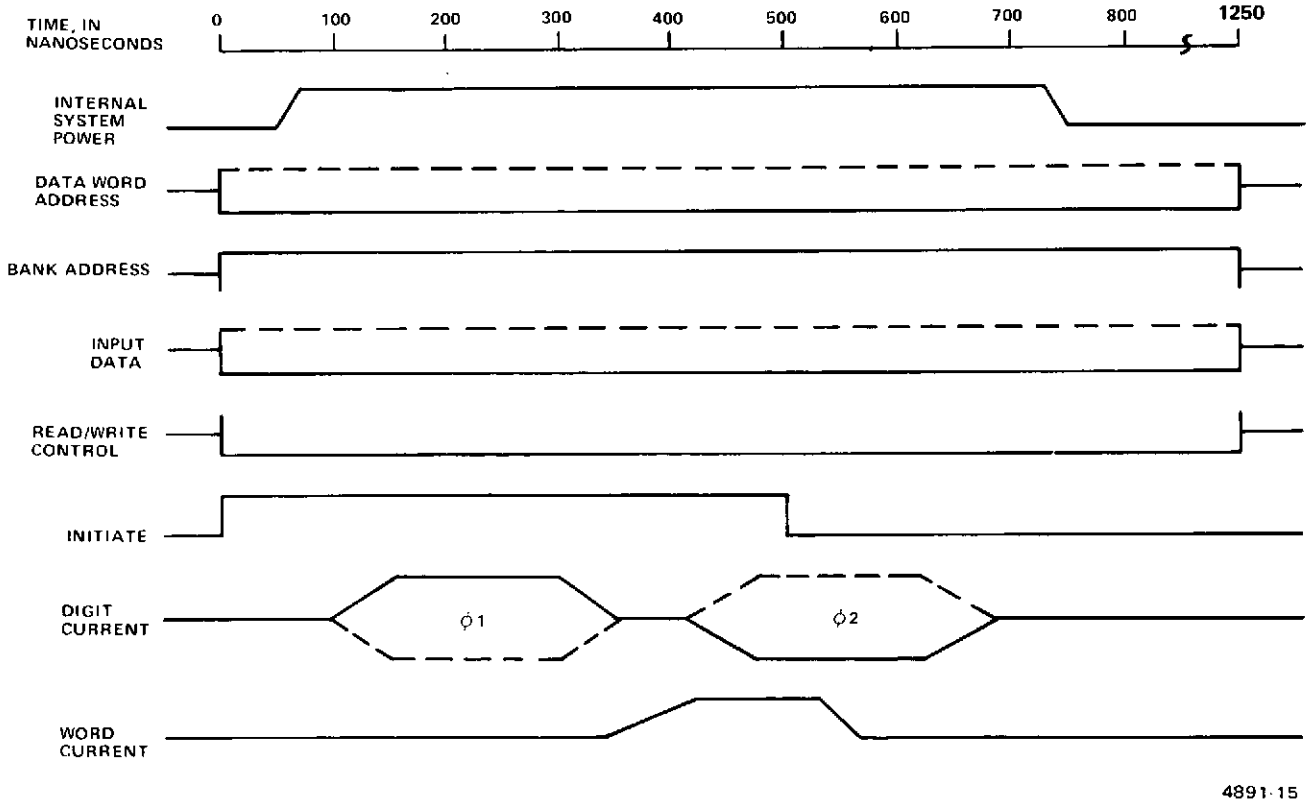

Figure 8. System Timing, Write Operation

The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when ϕ_2 digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the ϕ_2 digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in **Figure 9. For proper operation,** the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits 2^{10} and 2^{11}.

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously "written into" the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is clocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e. output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out (per Figure 2-9) of a bit 0.

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory.

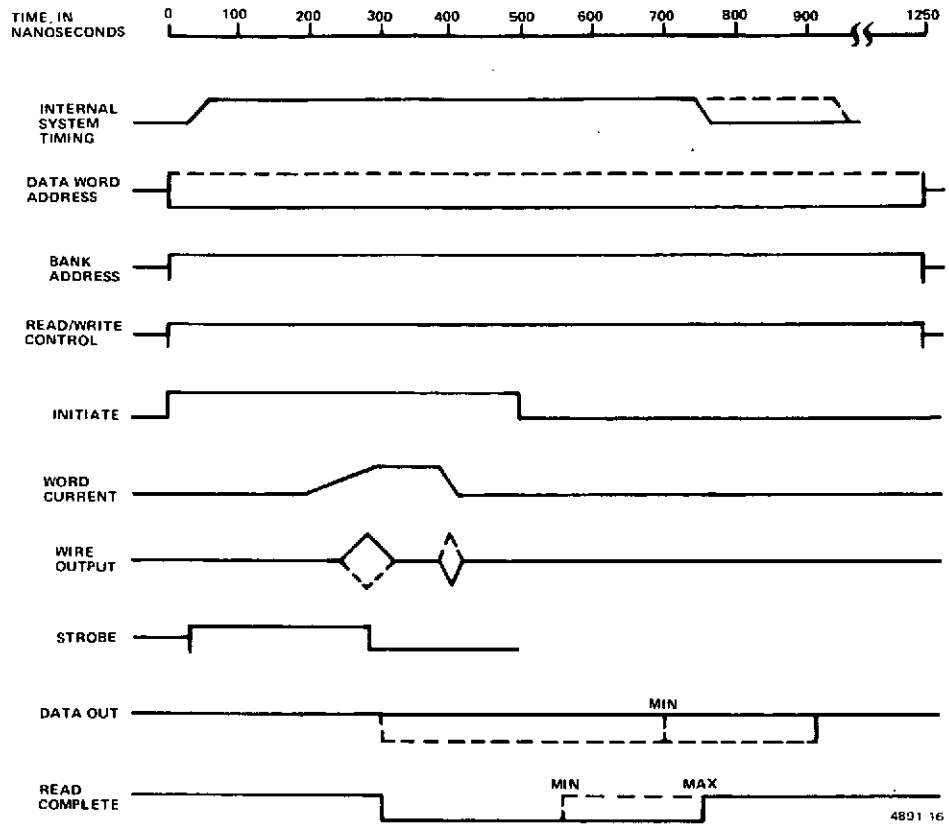

Figure 9. System Timing, Read Operation

3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. These were procured per vendor High-Rel specification SNC which is MIL-STD-883, Class B.

3.4.2 Discrete Parts

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. Both types were procured to S failure-rate levels.

Three types of capacitors were used; the CSR13 style, established reliability tantalum with failure rate of R or lower, the CKR05 and 06 style, established reliability ceramic with failure rate of R or lower, and the CM series mica per MIL-C-5/18 with additional screening for DWV and IR. Only JANTX transistors and diodes were used in construction of the memory.

3.4.3 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102, Condition C, except 10 cycles at -55°C.

3.4.4 Hybrid Circuits

Six different hybrids are used in the memory. These are custom circuits manufactured in-house and screened to meet the requirements of this program. Each of these circuits is described briefly in the following paragraphs.

3.4.4.1 Delay Circuit

The delay circuit is shown, functionally, in Figure 10. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.4.2 Word Current Generator

The word current generator is shown in Figure 11. It consists, basically, of a controlled current source for which the turn-on slope and the amplitude are programmable by selection of external, discrete components. The current is gated on and off by an external enable signal. Input voltages are monitored and the word current is inhibited if voltage(s) is below a level at which the memory will operate properly.

There is also a level detector on the current output from which a trigger is developed for sampling the sense amplifier outputs during a read operation.

3.4.4.3 Word-Line Selection Circuits

The word line selection circuits are shown in Figures 12 and 13. A particular switch is closed by grounding the corresponding selection input. The first and second level switches are packaged together. A particular package contains one first level switch and two banks of four second level switches each. Each of four second level selection inputs controls one switch in each bank. A single selection input controls the first level switch. The pin-outs are configured so that a first level switch can be connected to a second level bank in a different package, as well as to a bank in its own package.

3.4.4.4 Sense Amplifier

The four-channel sense amplifier (MC 1544) is shown in Figure 14. The input terminating resistors are external to the package.

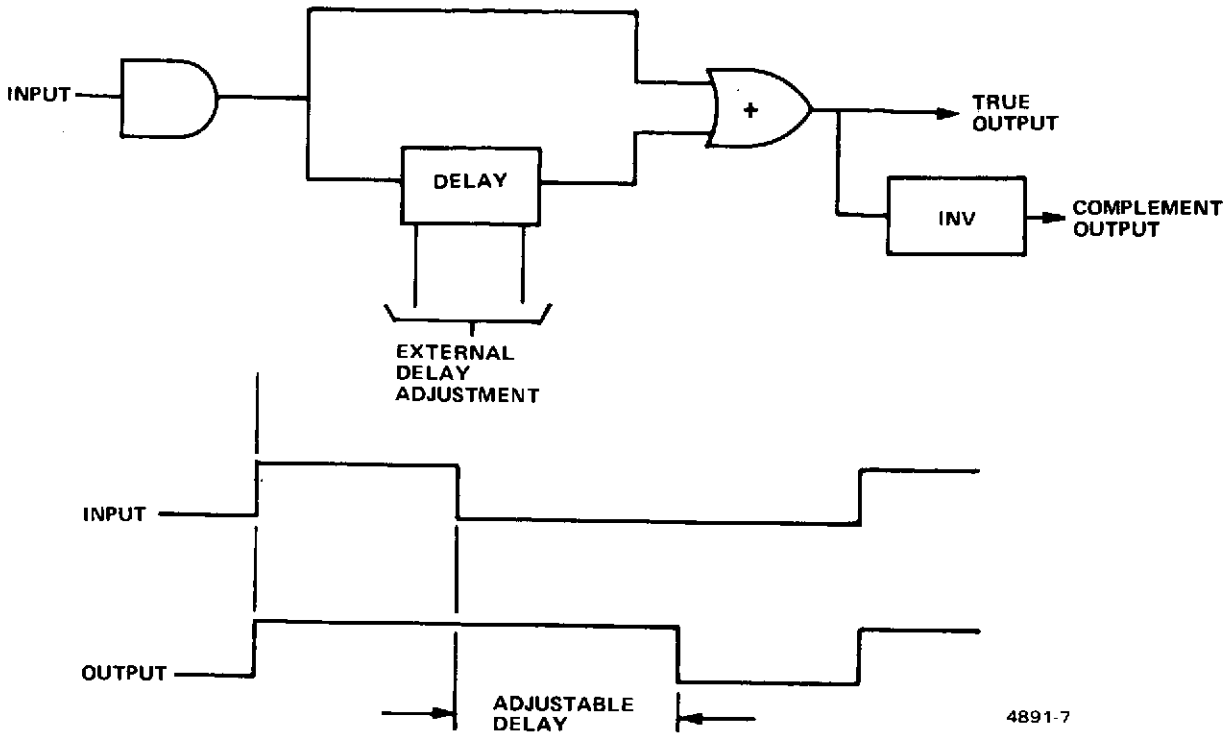

Figure 10. Delay Circuit, Functional Diagram

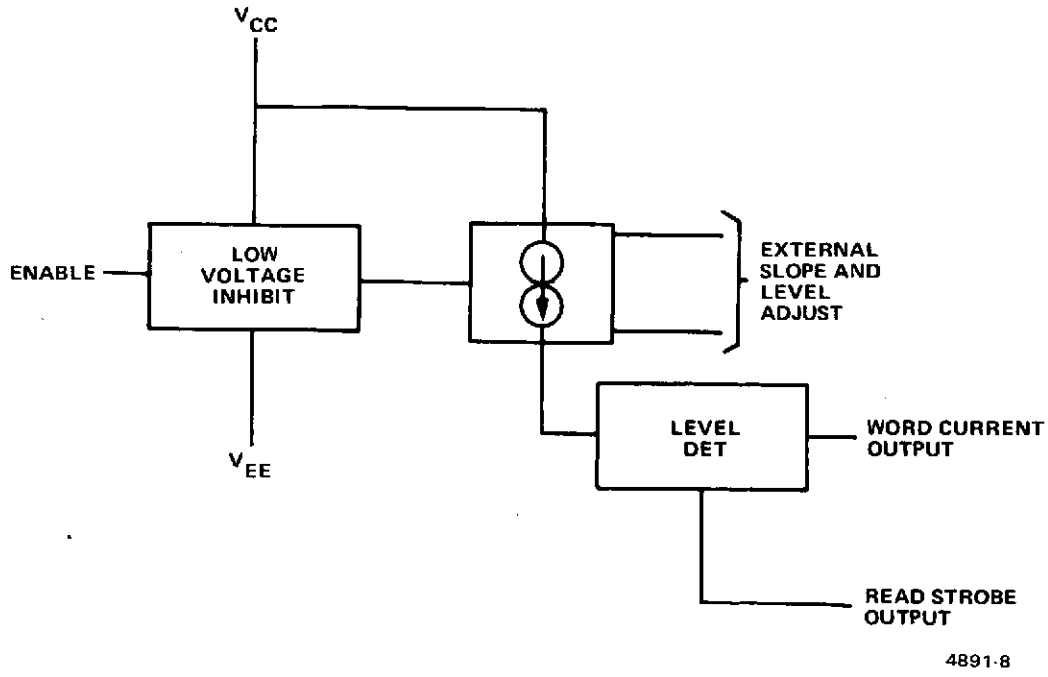

Figure 11. Word Current Generator, Functional Diagram

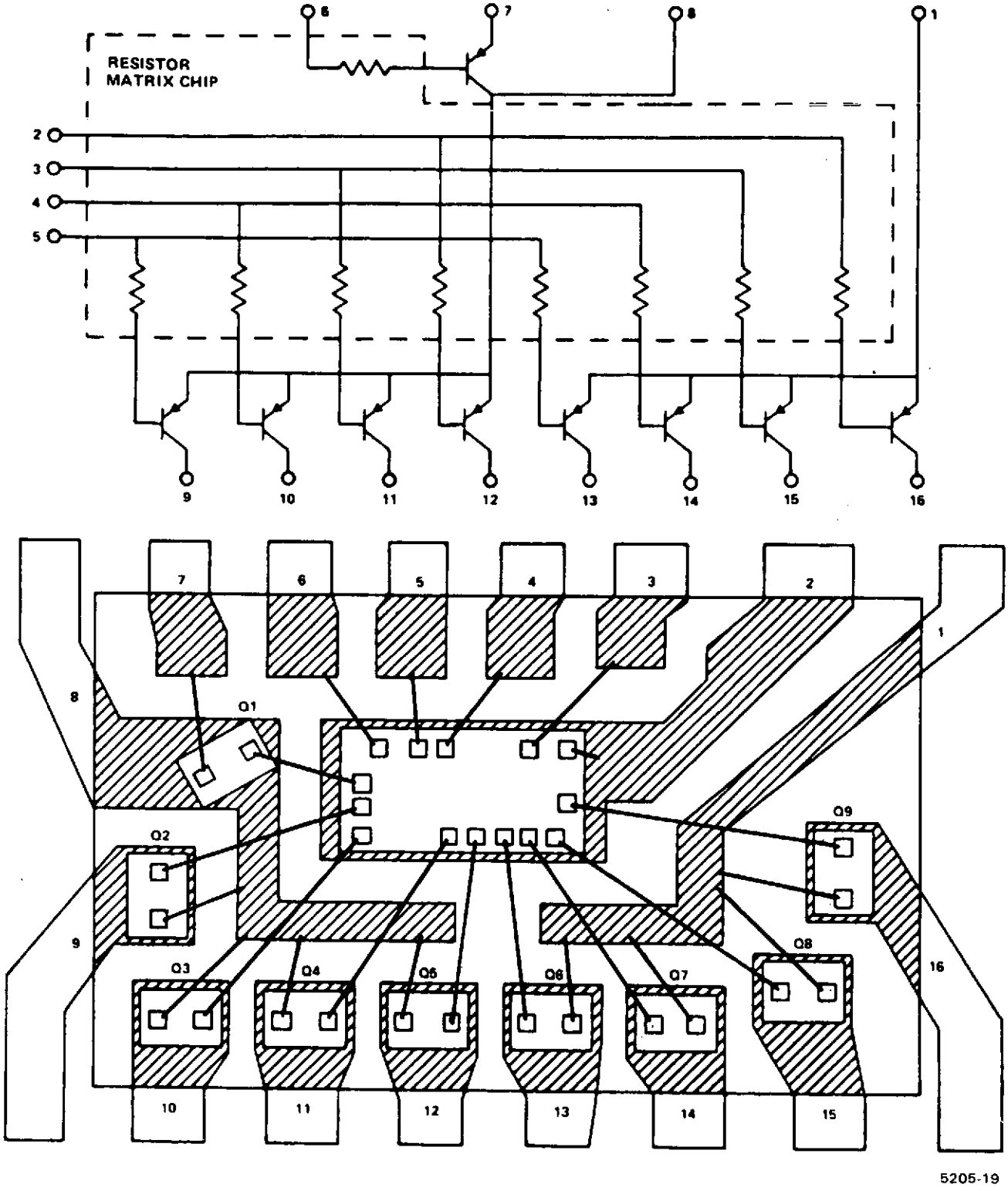

Figure 12. Custom Package and Layout

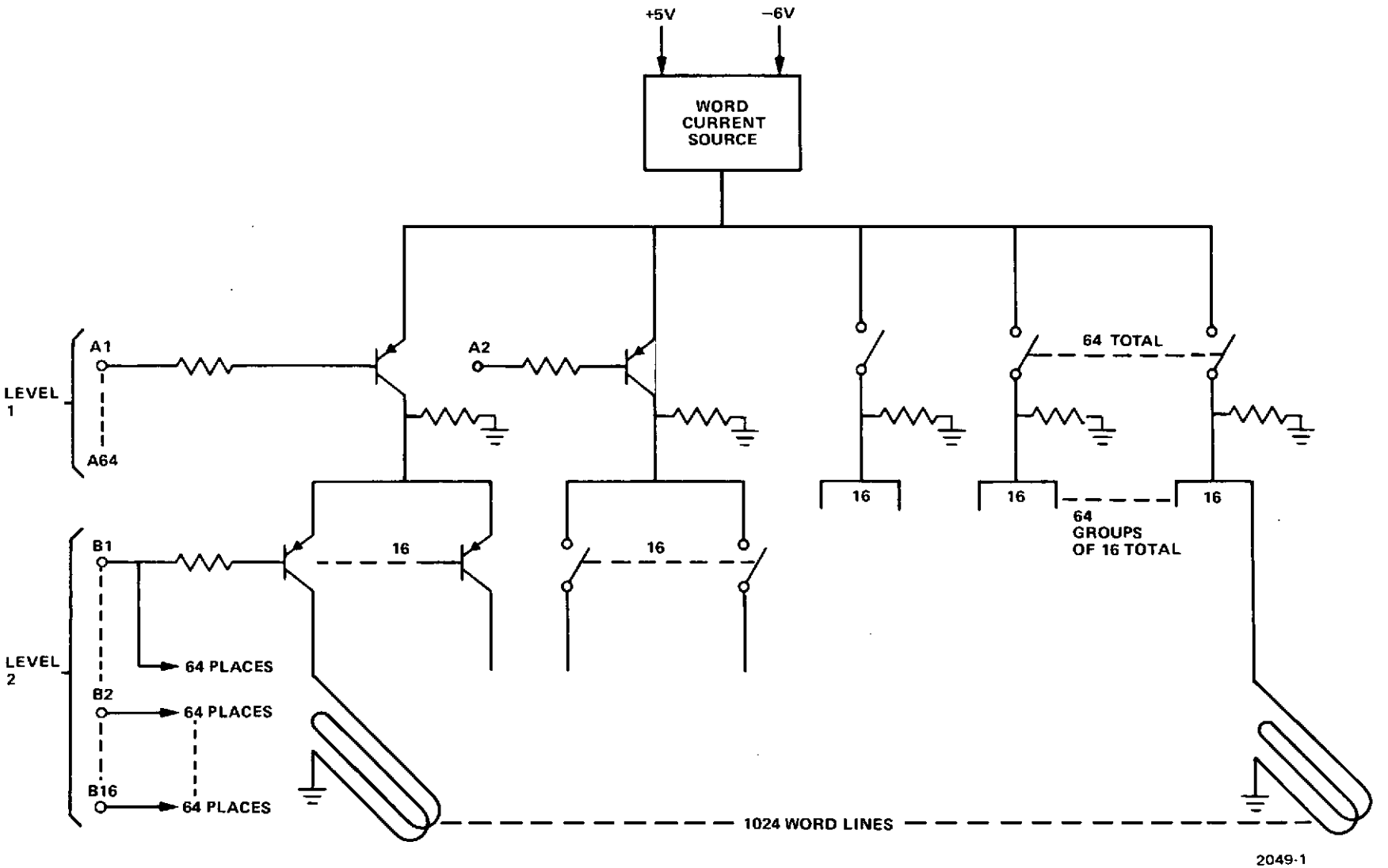

Figure 13. Word Line Selection Matrix, Functional Diagram

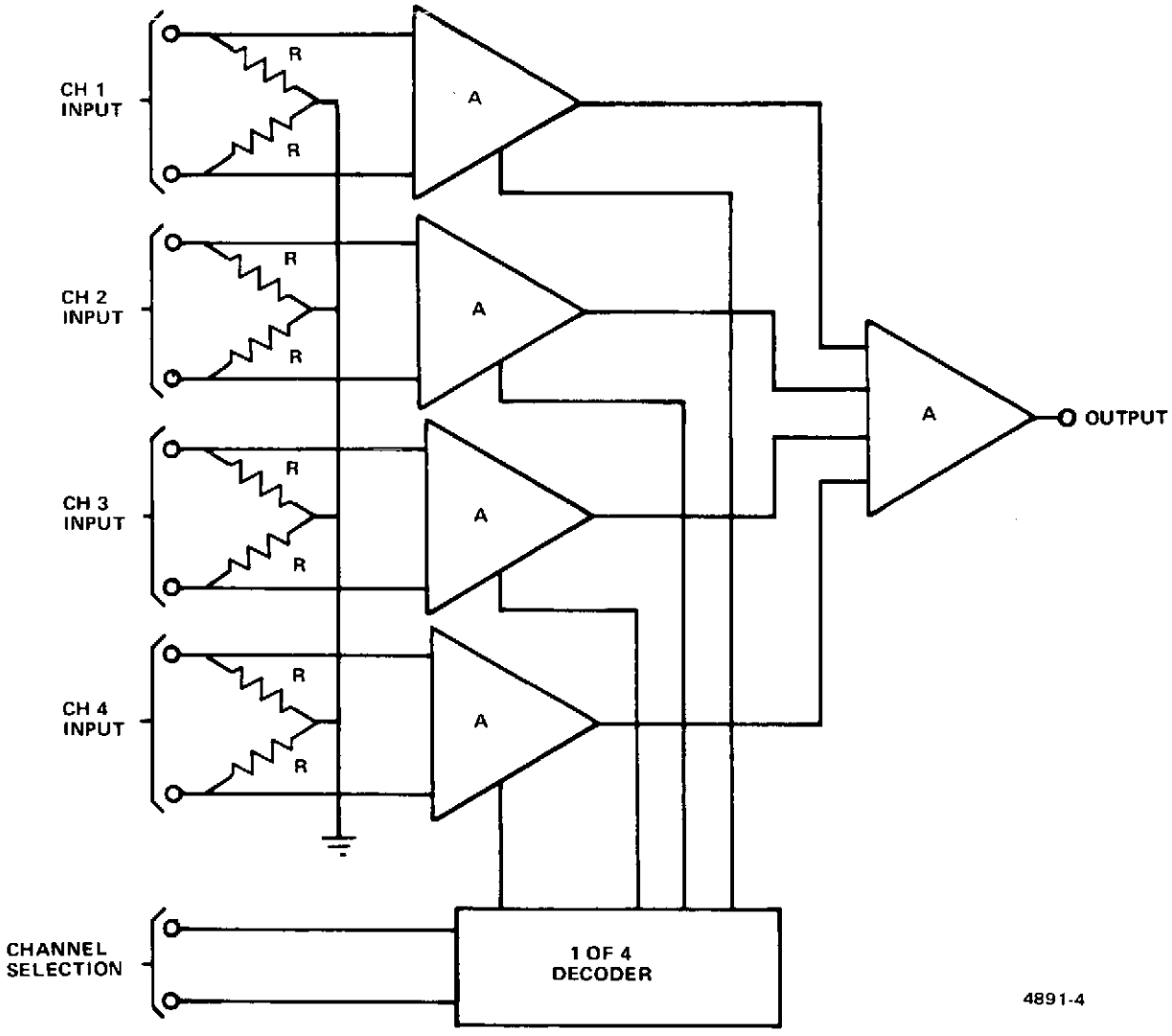

Figure 14. Four-Channel Sense Amplifier, Functional Diagram

3.4.4.5 Digit Driver

The digit driver is shown in Figure 15. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The T1 and T2 inputs denote successive time periods for the two opposite phases of digit current. The D and $\overline{D}$ inputs denote the true and complement levels of an input data bit. If D is true, then current will flow in the direction indicated during T1 and in the opposite direction during T2. The current flow would be opposite if $\overline{D}$ were true.

3.4.4.6 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.1 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 16 and 17.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.

The tunnel structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polymide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on glass epoxy board are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. Plated-thru holes at each end of the tunnel matt creates the double turn word lines.

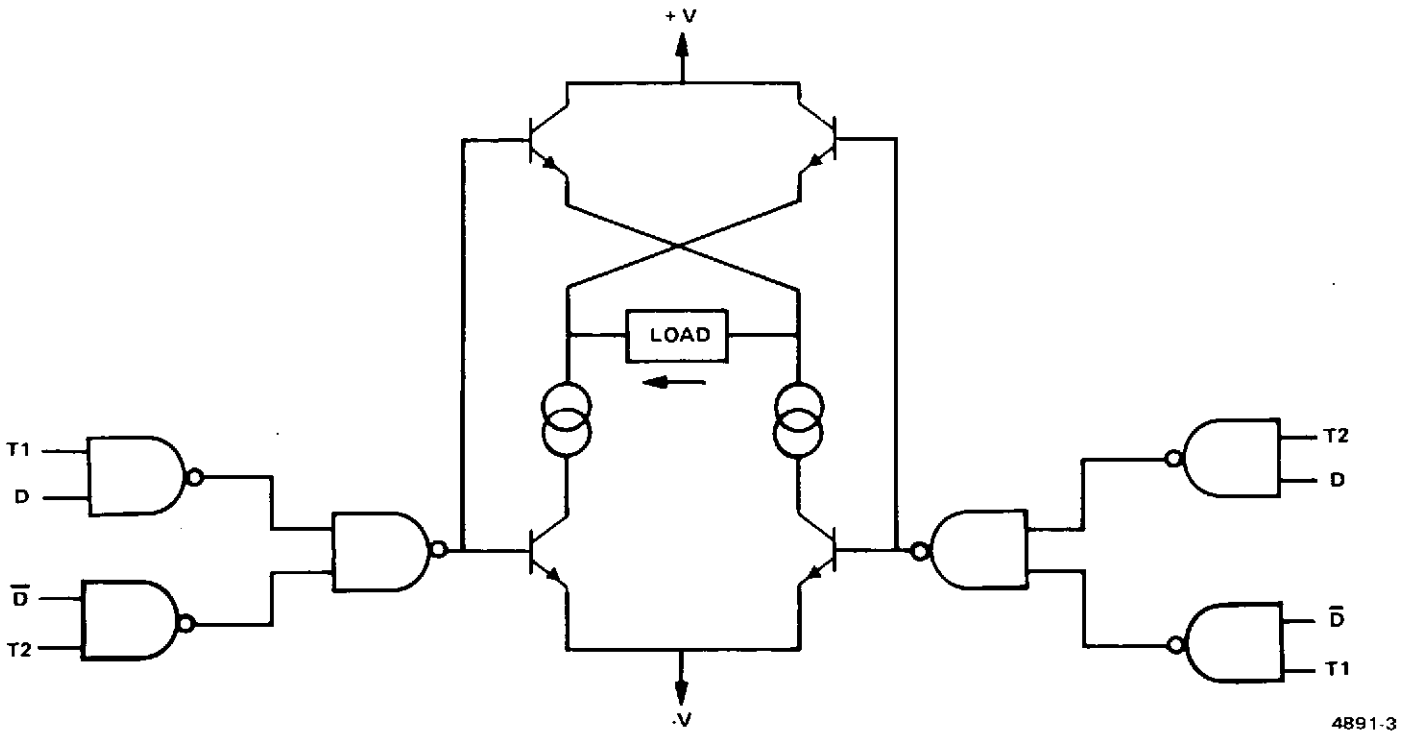

Figure 15. Digit Driver, Functional Diagram

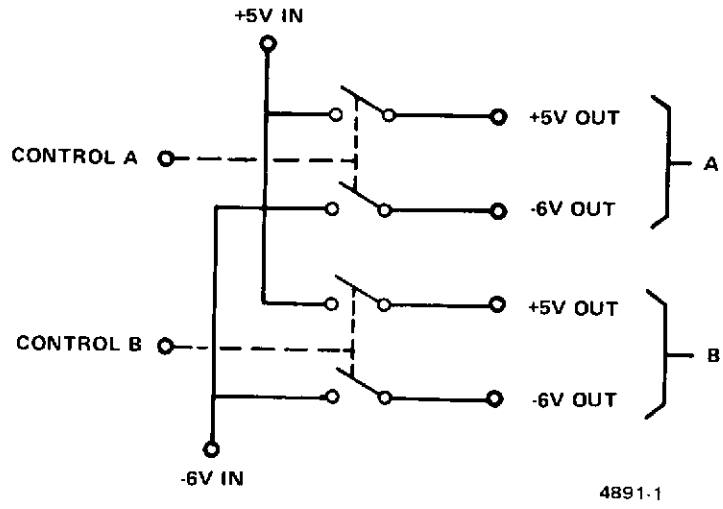

Figure 16. Power Switch +5V/-6V

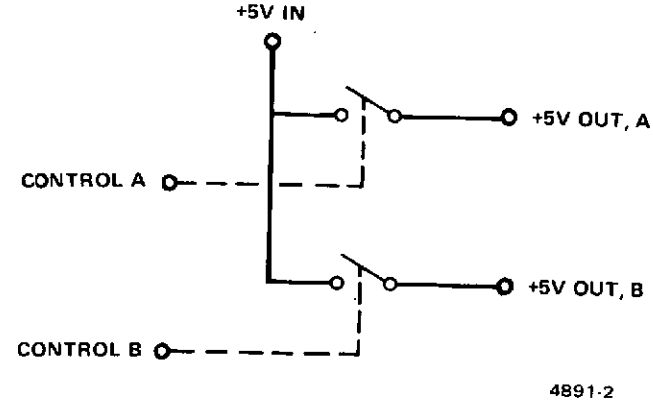

Figure 17. Power Switch +5V/+5V

Each carrier structure contains 64 word lines and 100 bit lines (Plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the glass epoxy board which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the tunnel structure is shown in Figure 18.

The memory plane is fabricated by laminating two tunnel structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a ground plane laminated in the center. The input and return for the matrix is tracked to the edge of the board where pc board interconnect is used to interface with the plane. Two tunnel structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly. Memory plane construction is shown in Figure 19.

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

PC board interconnect with miniature connectors (see Figure 2) is used to interconnect common word drive signals from plane to plane and carry all digit and word signals to the electronics. The use of printed circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.

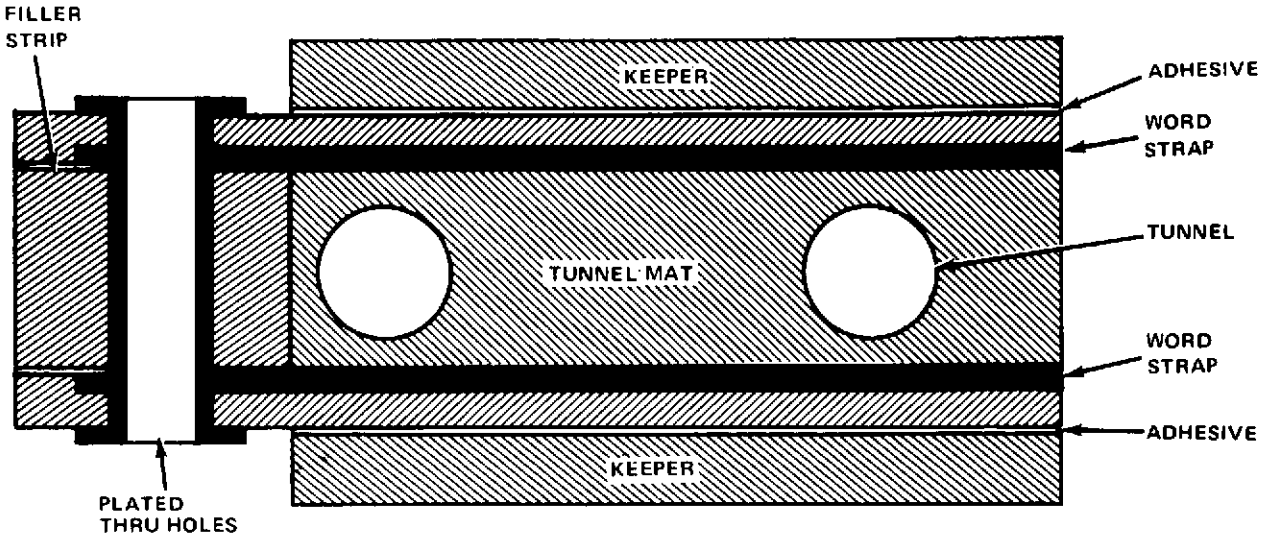

Figure 18. Tunnel Structure Construction

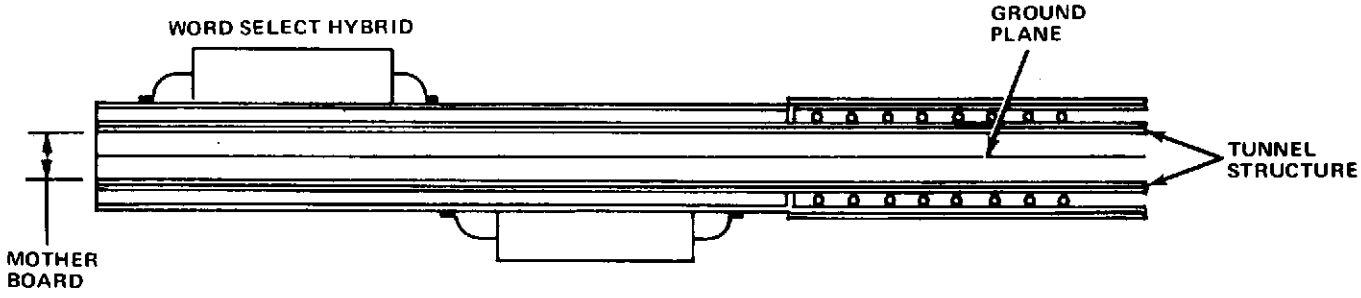

Figure 19. Memory Plane Construction

During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board is located on top of the plated wire stack while the two digit drive/sense boards are located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction.

The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.38" wide and contains 6 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 5.0" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Six special high strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from aluminum. The memory housing is 8.6" long x 6.3" wide x 2.9" high (exclusive of mounting flanges and connectors) establishing a volume of 157 cubic inches. The system has a total weight of 6.25 pounds.

3.5.3 Materials

Motorola's basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner '71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. The use of any material is dependent not only on the material but also on its receiving the proper processing and cure. This factor was considered in the assembly procedures and processes used to fabricate the memory system.

All of the material used in the LP RASM were submitted to the Chemistry and Physics Section of the Engineering Physics Division at GSFC for review and approval. From the preliminary design, some alternate materials were recommended and some changes in cure cycles were suggested. If data was not readily available on a material it was tested by the C&P Section to insure it met all requirements.

SECTION 4

TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its components at the piece part level and at each level of assembly. The formal test documents for tests performed at the stack and system levels are included as appendices.

4.1 SYSTEM LEVEL TESTING

Acceptance tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of $+85^{o}C$ and $-40^{o}C$. The Acceptance Test Procedure and Test Data Records are included as Appendix I. Acceptance Tests (except at high and low temperatures) were repeated after environmental testing.

Environmental testing consisted of both sine and random vibration, shock and altitude (to 10^{-5} mm Hg). The memory unit was continuously exercised during all environmental testing.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive, worst-case tests, over temperature, at the stack level using an EH8500 computer controlled stack tester. These tests were performed in accordance with a formal stack test procedure, which is included as Appendix II. The procedure is quite definitive, however, and some explanation is probably in order relative to the test pattern shown in Figure 8 (page 13 of the test procedure).

The first three horizontal rows relate to word current in the word line corresponding to the particular bit under test and word currents in the two word lines immediately adjacent (i.e., left adjacent bit and right adjacent bit). The fourth row relates to digit current in the plated-wire corresponding to the particular bit under test.

The vertical columns relate to successive time slots, left-to-right except that, as indicated in the row labeled NO. OF CYCLES, the first group of three time slots is cycled through 10^{3} times before stepping to the fourth time slot.

IWD identifies a maximum, or disturb, word current level. IWW and IWR identify a minimum word current level, which is worst-case for writing and reading in the bit-under-test. IDD1 and IDD2 identify maximum, or disturb, bipolar digit current levels. IDW1 and IDW2 identify minimum levels of the bipolar digit currents. These are worst-case for writing in the word-under-test.

During the first three time slots, information of a particular polarity is "hard-written" (i.e., under maximum word and digit current levels) into the bit-under-test and its two adjacent bits along the same plated-wire. This is done 1000 times and constitutes adverse history.

The opposite polarity information is then "soft-written" one time in the bit-under-test and then immediately read out, again with minimum word current. The resulting wire output represents an "undisturbed" condition (i.e., with no intervening activity at adjacent bit locations).

The next four program steps are cycled through a total of 10,000 times. During the first time slot, information opposite to that stored in the bit-under-test is written into one of the adjacent bits under conditions of worst-case maximum word and digit current levels. In the second time slot, maximum-level word current is pulsed through the word line corresponding to the bit-under-test. The same two steps are then repeated, only with reference to the other adjacent bit.

During the final time period, the bit-under-test is again read and compared to preset limits, using worst-case minimum word current.

Any wire which did not meet a minimum output level requirement of 4.5 millivolts, over temperature, was replaced. This amounted to a total of 56 wire pairs. There is a total of 576 wire pairs (72 pairs per plane times 8 planes) in the stack. The replacement incidence therefore represented less than 10 percent, which is well within normal expectations.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100 percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included precap visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging and leak testing.

APPENDIX I

ACCEPTANCE TEST PROCEDURES

* APPLICATION	
NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY -- FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	1-2-73	H. Tweed
X2	Incorporated changes prior to first usage.	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 10^{-6} mmHg to 10^{-5} mmHg. Change sine sweep levels, page 28. Change random vibration levels, page 29.	7-24-73	H. Tweed

REV	X1	X1	X1	X1	X1	X3																								
SHEET	27	28	29	30	31	32	33	34	35																					
REV STATUS	REV	X1	X1	X1	X1	X3	X1	X1	X1	X3	X1	X1	X3	X3	X1	X1	X1	X1	X1	X1	X3	X3	X3	X3	X3		X3			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG | PROJ NO. 4339

CONTR NO. NAS 5-23163

RELEASE NOTICE

APPROVED H. Tweed DATE 1-2-73

APPROVED DATE

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST PROCEDURE, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13722D 39

SCALE | SHEET 1 OF 35

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1. SCOPE

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13701D, manufactured under Contract No. NAS 5-23163.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory.
12-P13721D	Test Data Record
12-P11173B	Motorola Plated Wire Memory Tester Operating Manual.

2.2 DEFINITIONS

1	UP position on DATA and ADDRESS switches. DATA and ADDRESS lamps ON
0	DOWN position on DATA and ADDRESS switches. DATA and ADDRESS lamps OFF
Tester	Motorola Plated Wire Memory Tester
MSB	Most Significant Bit
LSB	Least Significant Bit
Error Lamps	Lamp ON indicates ERROR present.

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3. TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

ITEM	MANUFACTURER	MANUFACTURER'S MODEL OR TYPE	RANGE & ACCURACY
DC Milliammeter	Hewlett Packard	428B	0-10 Amp.
Oscilloscope	Tektronix	585	50ns/cm
Scope Plug-In	Tektronix	82	Tr 1.5ns
Digital Voltmeter	Hewlett-Packard	3440A	Accuracy ± .05% of reading
Counter	CMC	727BN	0.1% ± 1/2 LSB
DC Multifunction Unit	Hewlett-Packard	3444A	0-999.9 ma. 0-9.999 megohms
Oven	Wyle	CO-106-1800	-100°F to +500°F
Power Supplies	Precision Design Inc	5015-A	0-50V, 1.5 Amp.
Power Supplies	Precision Design Inc	5015-S	0-50V, 1.5 Amp.
Pulse Generator	EH	139B	10Hz to 50MHz

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NON-STANDARD TEST EQUIPMENT

(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-P11170B001

NOTE: The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE: The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull up resistor to signals coming back from the memory.

ENVIRONMENTAL TEST EQUIPMENT

ITEM	MANUFACTURER	MODEL NO.
Vibration Tester	LING	275
Vacuum Chamber	NRC	2707
Shock Tester	MRL	2424
Vibration Test Fixture	MOT	—

3.2 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions.

3.2.1 Power Supply Voltage

The unit specified to be tested shall operate from the following DC source voltages:

+5.0V ± 5%
-6.1V ± 5%

3.2.2 Ambient Temperature

The unit shall be tested in a laboratory area having a temperature of +25 ± 10°C (77 ± 18°F).

3.2.3 Ambient Humidity

Normal laboratory ambient, not to exceed 90%.

3.2.4 Ambient Atmospheric Pressure

Normal laboratory ambient.

3.2.5 Stabilization Period

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4. TEST SCHEDULE

The testing to be performed on each memory unit is as follows:

1. Physical Characteristics (Weight and Dimensions)
2. Comprehensive Initial Functional Tests
3. Operational Tests at Temperature Extremes
4. Operational Vacuum Tests
5. Operational Vibration Tests
6. Operational Shock Tests
7. Final Functional Tests

Tests 3 through 6 may be performed in any sequence.

5. TEST RECORDS

5.1 TEST LOG

The Test Log shall be used to record the history of the memory, starting from the first system test. The log shall reference all testing, rework and idle time for the particular memory unit.

5.2 DATA RECORD

All test results shall be recorded in the Test Data Record, Motorola Document No. 12-P13721D.

6. PHYSICAL CHARACTERISTICS

6.1 WEIGHT

Place the LP RASM on the scale and read and record, in the data sheet, the weight of the memory, in pounds.

6.2 DIMENSIONS

Measure and record, in the data sheet, the outside dimensions as shown in Figure 1. Compute and record, in the data sheet, the memory volume by multiplying dimension W by dimension H by dimension D. (V = W X H X D).

7. INITIAL FUNCTIONAL TESTS

7.1 INTERCONNECTION

At the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The

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connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for +3 ± 0.1V positive pulses of 450 ± 10 nanosecond duration (at the 50 percent points) at a 500 ± 1.0 KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

7.2 PRELIMINARY CONTROL SETTINGS

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
TESTER	
BD1-BD4(24 Switches)	No. 0 Down all Other Up
Tape Reader Power	Light Off
Run-Off-Rewind Switch	OFF
Tester Power	Light On
Address Switches	Down

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CONTROL	SETTING
TESTER (Cont.)	
Data Switches	Down
READ/WRITE	WRITE
Word Length	24
READ 1/ READ 7 Switch	READ 1
Address Pattern	SEQ.
Data Pattern	MAN
Frequency	EXT.
INTERFACE BOX	
Memory Select Switches	All 2.4V
Input Current Switch	GND
Output Pullup Resistor	GND
WC Switch	OFF
Initiate Pulse Switch	GND
WC2 Switch	OFF
Memory Power	OFF

7.3 INITIAL POWER SUPPLY CONDITIONS

Using the DVM, adjust the three supplies as follows:

+5V to Interface Box: +5.0V $\pm$ 0.1V

+5V to Memory: +5.0 $\pm$ 0.1V

-6.1V to Memory: -6.1 $\pm$ 0.1V

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Set the meter selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

7.4 CHASSIS ISOLATION

Using the digital ohmmeter verify that the impedance between the memory chassis and ground test point on the interface box is $\geq$ 9 megohoms. Record the results in the Data Sheet.

7.5 INPUT SIGNAL LOADING

7.5.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).

7.5.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.

7.5.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter. Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position.

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Momentarily set MEMORY POWER to ON and measure and record the current.

Disconnect the ammeter and replace the jumper wire. Set the MEMORY SELECT 1 SWITCH back to the +2.4V position.

7.5.4 Repeat paragraph 7.5.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.

7.5.5 Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.

7.5.6 Connect the ammeter between the ADDRESS BIT 2^{0} and the INPUT CURRENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current.

Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.

Repeat the above two measurements at each of the 12 address bit test points. Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).

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Verify that the MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS.

7.6.1 Connect the Interface Box to the tester. Connect the -6.1V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons.

7.6.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "0" in all data bits in all 4096 addresses one time and stop.

7.6.3 Set the READ/WRITE switch on the tester to the READ position. Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be $\leq$100 mv.

(The read complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

7.6.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be $\leq$100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.

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7.7 POWER CONSUMPTION

7.7.1 Using the DVM, adjust the +5V and -6.1V memory power supplies to +5.0 ± 0.1V and -6.1 ± 0.1V, respectively. Record the voltages.

Using the 428B milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

7.7.2 Using the milliammeter, measure and record the current to the -6.1V supply. Compute and record the -6.1V power.

7.7.3 Compute and record the total Memory Idle Power.

7.7.4 Set the ADDRESS PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.

7.7.5 Repeat 7.7.1.

7.7.6 Repeat 7.7.2.

7.7.7 Compute and Record the Total Active Power.

7.8 READ COMPLETE TIMING

7.8.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to the INITIATE PULSE test point and the channel B voltage probe to the READ COMPLETE test point.

7.8.2 Set the DATA PATTERN switch to MAN and the READ/WRITE switch to READ.

7.8.3 Depress and release the RESET button, then the START button.

7.8.4 Synchronize the oscilloscope on the leading edge of the initiate pulse.

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7.8.5 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points). Record the pulse delay and duration in the data sheet.

7.8.6 Momentarily depress the STOP button and set the READ/WRITE switch to WRITE. Depress and release the RESET button, then the START button. Set the READ/WRITE switch to READ and momentarily depress the START switch.

7.8.7 Connect the scope channel A voltage probe to the first data output line test point (DO-0). The high-to-low transition on the data output line shall occur prior to (or in coincidence with) the leading edge of the read complete pulse. The low-to-high transition of the data output line shall occur no earlier than 150 nanoseconds following the trailing edge of the read complete pulse. (All timing relationships shall be measured at the 50 percent points). Record the results.

7.8.8 Repeat the measurements of 7.8.7 at each of the remaining 17 data output line test points. Record the results.

7.9 SYSTEM FUNCTIONAL TESTS

7.9.1 Depress and release the RESET button. Set the ADDRESS PATTERN switch to SEQ. Adjust the pulse generator frequency to 600 ± 1.0 KHz.

Set the DATA PATTERN switch to SEQ.

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7.9.2 Depress and release the START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1" and reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs.

Test for 10 seconds and record any errors. Use the counter to measure the elapsed test time. Depress the STOP button.

7.9.3 Set the READ 1/READ 7 Switch to the READ 7 position. The READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "1", and read a "1" seven times in each memory location.

7.9.4 Depress and release the START button. The Tester will continue to cycle unless an error occurs.

Test for 10 seconds and record any errors.

7.9.5 Depress and release the STOP button. Set the DATA PATTERN switch to MAN and the READ/WRITE switch to WRITE. Set all DATA switches to the DOWN position.

7.9.6 Depress and release the RESET button and then the START button.

7.9.7 Set all DATA switches to the UP position.

7.9.8 Depress and release the RESET button and then the START button.

7.9.9 Set the READ/WRITE switch to READ. Depress and release the RESET button.

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7.9.10 Depress and release the START button. Test for one minute. Record any errors.

7.9.11 Depress and release the STOP button.

7.9.12 Set the READ/WRITE switch to WRITE.

7.9.13 Set all DATA switches to the DOWN position. Depress and release the RESET button.

7.9.14 Depress and release the START button. The memory will cycle thru all 4096 addresses one time and stop.

7.9.15 Set the READ/WRITE switch to READ. Depress and release the RESET button.

7.9.16 Depress and release the START button. Run for one minute. Record any errors.

7.9.17 Depress and release the STOP button.

7.10 RANDOM ACCESS CAPABILITY

7.10.1 Set the READ/WRITE switch to WRITE and the ADDRESS PATTERN switch to MAN.

7.10.2 Select an address at random with the ADDRESS switches.

7.10.3 Set the DATA switches in a random pattern. Depress and release the RESET button.

7.10.4 Depress and release the START button. The selected data will be written into the selected address.

7.10.5 Depress and release the Stop button. Set the READ/WRITE switch to READ.

7.10.6 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.

7.10.7 The operator should select 3 other addresses at random, repeating steps 7.10.2 through 7.10.6 to verify the random access capability.

7.11 NON-VOLATILITY TEST

7.11.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to MAN.

7.11.2 Set the DATA switches to a random pattern. Depress and release the RESET button. Set the READ/WRITE switch to WRITE.

7.11.3 Depress and release the START button. The tester will run through all 4096 addresses one time and then stop. Set the READ/WRITE switch to READ.

7.11.4 Turn memory power to OFF.

7.11.5 Depress and release the RESET button.

7.11.6 Turn memory power to ON.

7.11.7 Depress and release the START button. If any errors occur, record them on the data sheet. If no errors occur, no words were disturbed when the power was interrupted.

7.11.8 Depress and release the STOP button.

7.11.9 Repeat 7.11.4 through 7.11.8 four times. Record any errors.

7.12 MEMORY SELECT TEST

7.12.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to SEQ.

7.12.2 Set the MEMORY SELECT switches to 0000.

7.12.3 Depress and release the RESET button, then the START button. The tester should indicate an error at the first address. Record this address on the data sheet.

7.12.4 Repeat 7.12.3 with the memory select switches set to 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, and 1110.

7.12.5 Set the MEMORY SELECT switches to 1111.

7.12.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow the tester to run for 10 seconds. Record any errors. Depress and release the STOP button.

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SCOTTSDALE, ARIZONA 85252

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13722D

SCALE	REVISION	SHEET 18

7.13 WORST CASE PATTERN TEST

7.13.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WC1. Turn the WC switch ON. Depress and release the STOP and RESET buttons.

7.13.2 Depress and release the START button. The tester will execute the following sequence:

A. Write a "1" in every bit of every word 2^{10} times.

B. Write a "0" once in every bit of every word under an even numbered word line in the stack.

C. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.

NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worst-case pattern tests.

Run in cycle C for one minute. Record any errors on the data sheet.

7.13.3 Press and release the WC1 SEQ button. The tester will execute the preceeding sequence, except "even" and "odd" are interchanged. The $WC2^0$ and $WC2^1$ lights will indicate the second WC1 group is under test. Record any errors.

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7.13.4 Repeat 7.13.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet. Depress and release the STOP button. Turn the MEMORY POWER to OFF.

8. TEMPERATURE TEST

The temperature tests shall be conducted under normal laboratory conditions, with the exception of temperature.

8.1 TEST SETUP

Place the unit in the temperature chamber and establish the test setup as shown in Figure 3.

8.2 HIGH TEMPERATURE

Increase the chamber ambient temperature to $+85^{\circ} \pm 3^{\circ}C$. When the chamber has reached this temperature, note the time and set the DATA PATTERN and ADDRESS PATTERN switches to WC1. Turn the WC switch to ON. Turn MEMORY POWER to ON and depress the START button. Using the DVM, adjust the memory power supplies to $+5.25 \pm 0.02V$ and $-6.40 \pm 0.02V$. Depress the STOP button.

8.2.1 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.2.2 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to $+4.75 \pm 0.02V$ and $-5.80 \pm 0.02V$. Depress the STOP button.

8.2.3 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.2.4 Beginning 50 minutes after the temperature chamber has reached $85^{\circ}C$ measure and record, on the data sheet, the thermistor resistance at 10 minute intervals. Do this by connecting the

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digital ohmmeter across the THERMISTOR terminals on the interface box. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent, proceed to paragraph 8.2.5.

8.2.5 Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ. Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Measure and record the power supply voltage, current and standby (idle) power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages).

8.2.6 Depress the START button. The memory shall run without error for 10 seconds. Record the results.

8.2.7 Adjust the pulse generator frequency to 500 ± 1.0 KHz. Measure and record the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to +5.25 ± 0.02V and -6.40 ± 0.02V). Depress the STOP button. Adjust the pulse generator frequency to 600 ± 1.0 KHz.

8.2.8 Repeat paragraphs 7.13.1 through 7.13.4.

8.2.9 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +4.75 ± 0.02V and -5.80 ± 0.02V. Depress the STOP button,

8.2.10 Repeat paragraphs 7.13.1 through 7.13.4.

8.2.11 Set the MEMORY POWER switch to ON.

Set the +5V supply to 5.0V ± .02 and the -6.1V and to -6.1 ± .02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory shall run without error. After 10 seconds, push the STOP button. Record the results. Set MEMORY POWER to OFF.

8.3 LOW TEMPERATURE

Remove the oven door and let the memory unit cool to approximately room temperature. Place the memory unit in a plastic bag and again seal the chamber.

8.3.1 Decrease the chamber ambient temperature to $-40^{\circ} \pm 3^{\circ}C$. When the chamber has reached this temperature, note the time. Monitor the thermistor resistance by connecting the digital ohmmeter across the THERMISTOR terminals on the interface box. When the termistor resistance has reached 29 Kohms, proceed to paragraph 8.3.2.

8.3.2 Set the DATA PATTERN and ADDRESS PATTERN switches to WC1. Turn the WC switch to ON. Turn MEMORY POWER to ON and depress the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Depress the STOP button.

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8.3.3 Ropeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.3.4 Set the MEMORY POWER switch to ON. Depress the START button. Using the DVM, adjust the memory power supplies to +4.75 ± 0.02V and -5.80 ± 0.02V. Depress the STOP button.

8.3.5 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.3.6 Beginning 150 minutes after the chamber temperature has reached -40°C, measure and record, in the data sheet, the thermistor resistance at 10 minute intervals. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent proceed to paragraph 8.3.7.

8.3.7 Depress the START button. The memory shall run without error for 10 seconds. Depress the STOP button and record the results.

8.3.8 Set the +5V supply to 5.25V ± .02V and the -6.1V supply to -6.40 ± .02V. Measure and record the power supply volt & the standby power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages).

8.3.9 Adjust the pulse generator frequency to 500 ± 1.0 KHz. Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record, in the data sheet, the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to +5.25 ± 0.02V and -6.40 ± 0.02V).

. . . Adjust the pulse generator frequency to 600 ± 1.0 KHz.

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8.3.10 Set the +5V supply to +4.75 ± .02V and the -6.1V supply to -5.80 ± .02V. Push the RESET pushbutton. The memory shall run without error for one minute. Depress the STOP button. Record the results in the data sheet.

8.3.11 Repeat paragraphs 7.13.1 through 7.13.4.

8.3.12 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and - 6.40 ± 0.02V. Depress the STOP button.

8.3.13 Repeat paragraphs 7.13.1 through 7.13.4.

8.3.14 Turn the memory power OFF.

9. VACUUM TEST

9.1 SETUP

9.1.1 Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the coarse voltage controls fully counter-clockwise on all three power supplies.

Connect the equipment as shown in Figure 3.

Turn on power to all memory associated test equipment.

9.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
TESTER	
BD1-BD4 (24 Switches)	UP
Tape Reader Power	Light Off
Run-OFF-Rewind Switch	OFF
Tester Power	Light ON
ADDRESS Switches	DOWN
DATA Switches	DOWN
READ/WRITE	READ
WORD LENGTH	24
READ 1/READ 7 Switch	READ 7
ADDRESS PATTERN	SEQ
DATA PATTERN	SEQ
FREQUENCY	EXT
INTERFACE BOX	
MEMORY SELECT SWITCHES	All 2.4V
INPUT CURRENT SWITCH	GND
OUTPUT PULLUP RESISTOR	+5V
INITIATE PULSE SWITCH	PULSE
WC2 SWITCH	OFF
WC SWITCH	OFF
MEMORY POWER	OFF

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9.1.3 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to +5.0 ± 0.1V. Set the memory supplies to approximately +5V and -6V. Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to +5.0 ± 0.1V and -6.1 ± 0.1V. Set the memory power switch to OFF.

9.1.4 Using the scope, adjust the Pulse Generator for +3.0 ± 0.1V positive pulses of 450 ± 10 nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to 600 ± 1.0 KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.

9.2 TEST

Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors. Proceed immediately to paragraph 9.2.1.

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9.2.1 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vacuum chamber at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors.

9.2.2 Continue pumping the chamber until the pressure 10^{-5} mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF and turning the TESTER POWER OFF. After the chamber has reached 10^{-5} mmHg, test the memory as outlined in paragraph 7.13. Record any errors. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, turn the TESTER POWER OFF and return the memory to one atmosphere pressure.

10. VIBRATION TEST

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis

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shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

10.1 SINE SWEEP TEST

10.1.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 3 and turn on power to all memory associated test equipment.

Perform paragraphs 9.1.2, 9.1.3, and 9.1.4.

Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 4. (The axis order may be varied for convenience).

10.1.2 Push the STOP and RESET buttons. Turn the MEMORY POWER ON. Perform a sine sweep over the fequency range of 5-2000 Hz at the levels listed below:

FREQUENCY RANGE	TEST LEVEL
5-25 Hz	0.33 in DA
24-110 Hz	10G PEAK
110-2000 Hz	5g PEAK

The sweep rate is to be 2 octaves per minute. During the sweep, repeatedly perform the tests of paragraph 7.13. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.

10.2 RANDOM VIBRATION

10.2.1 Perform the spectral analysis specified in paragraph 10. While applying the following random vibration input, repeatedly perform the tests of paragraph 7.13.

FREQUENCY RANGE	TEST LEVEL	TOLERANCE
15 Hz	.0044 g^2/Hz	± 3db
15-70 Hz	LINEAR INCREASE	Log-Log Plot
70-1000 Hz	.138 g^2/Hz	± 3db
100-400 Hz	LINEAR DECREASE	Log-Log Plot
400-2000 Hz	.0089 g^2/Hz	± 3db

The test time is to be 2 minutes per axis.

Record any errors in the Data Record.

10.22 Repeat paragraph 10.1.2 and 10.2, in the two other mutually perpendicular axes as shown in Figure 4. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

11. SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

11.1 SETUP

Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3 and apply power to all memory associated test equipment. Set the controls as shown in para. 9.1.2 and perform para. 9.1.3 and 9.1.4. Mount the LP RASM on the shock table so as to apply

the shock in the vertical (Y) axis as shown in Figure 5. (The axes order may be varied for convenience).

11.2 TEST

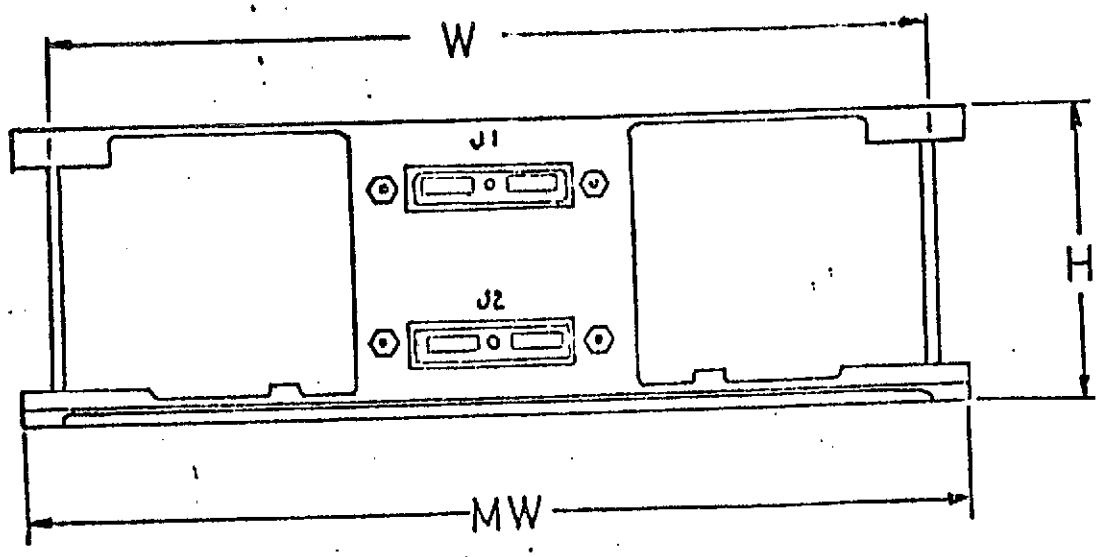
11.2.1 Push the STOP and RESET buttons. Turn the MEMORY POWER ON and push the START button. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors. Push the STOP button.

11.2.2 Push the RESET and START buttons. Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors.

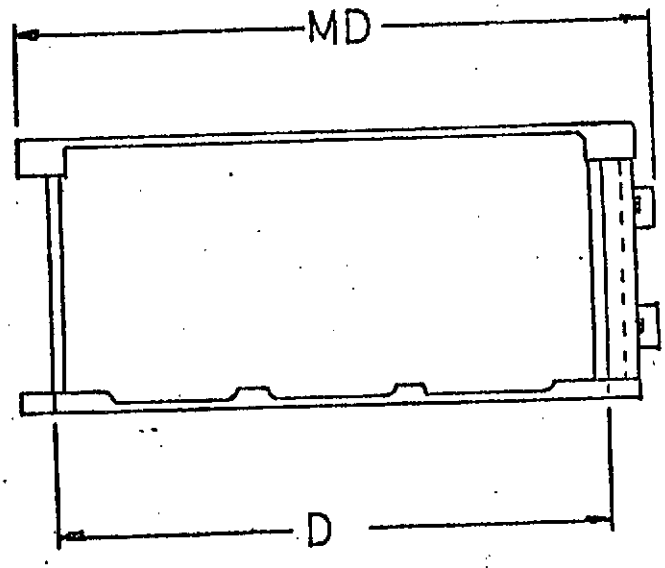
11.2.3 Repeat para. 11.2.1 and 11.2.2 for each of the other two directions as shown in Figure 5. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

12. FINAL FUNCTIONAL TESTS

To insure that the memory is still operating properly, perform all the tests of paragraph 7. Record the data.



FRONT



SIDE

FIGURE 1. LP RASM OUTLINE DIMENSIONS

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13722D
	SCALE NONE	REVISION	SHEET 31

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V-2-B-1911-10A-3.69 DWG FORMAT

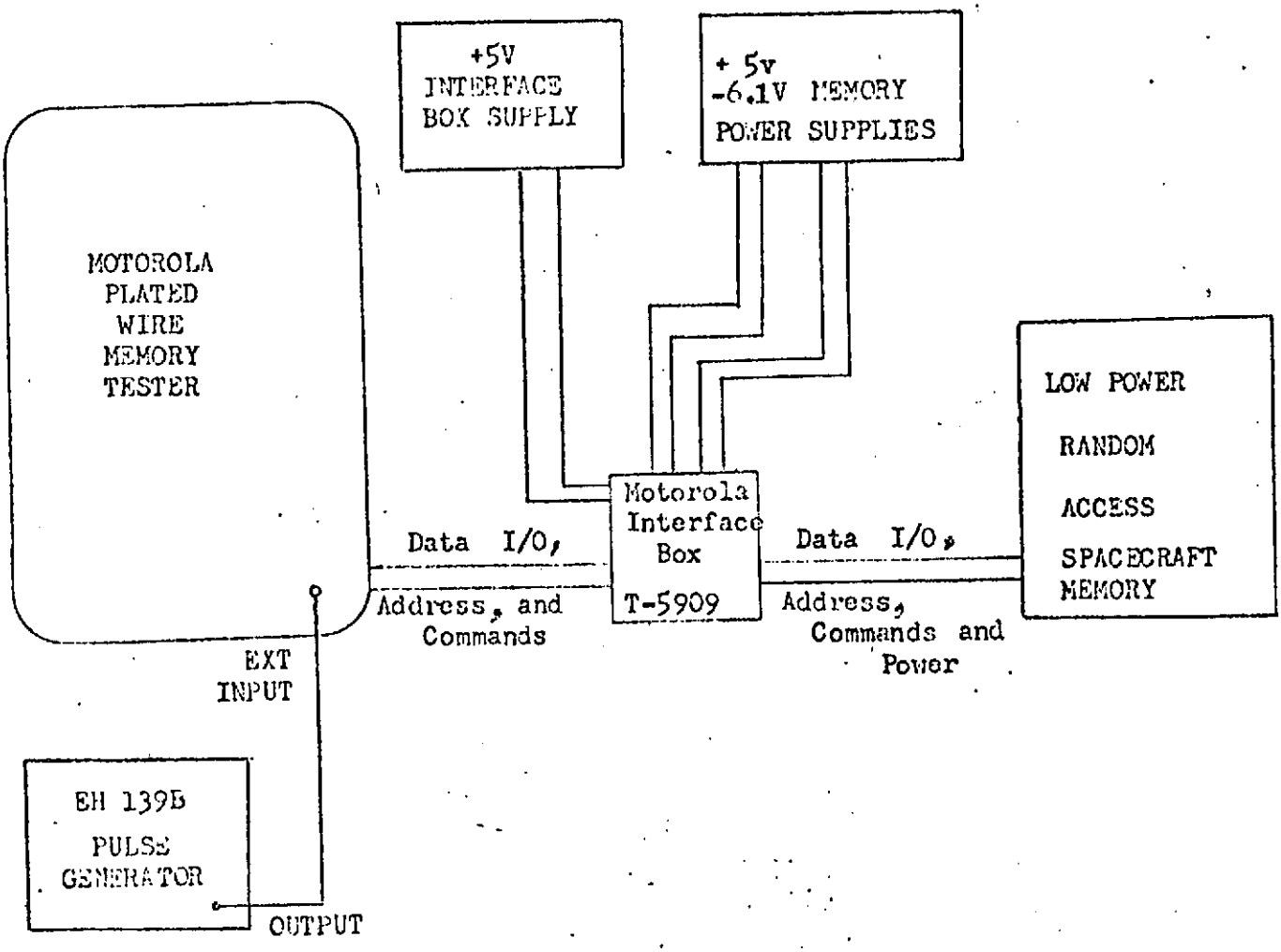


FIGURE 2. TEST SET UP

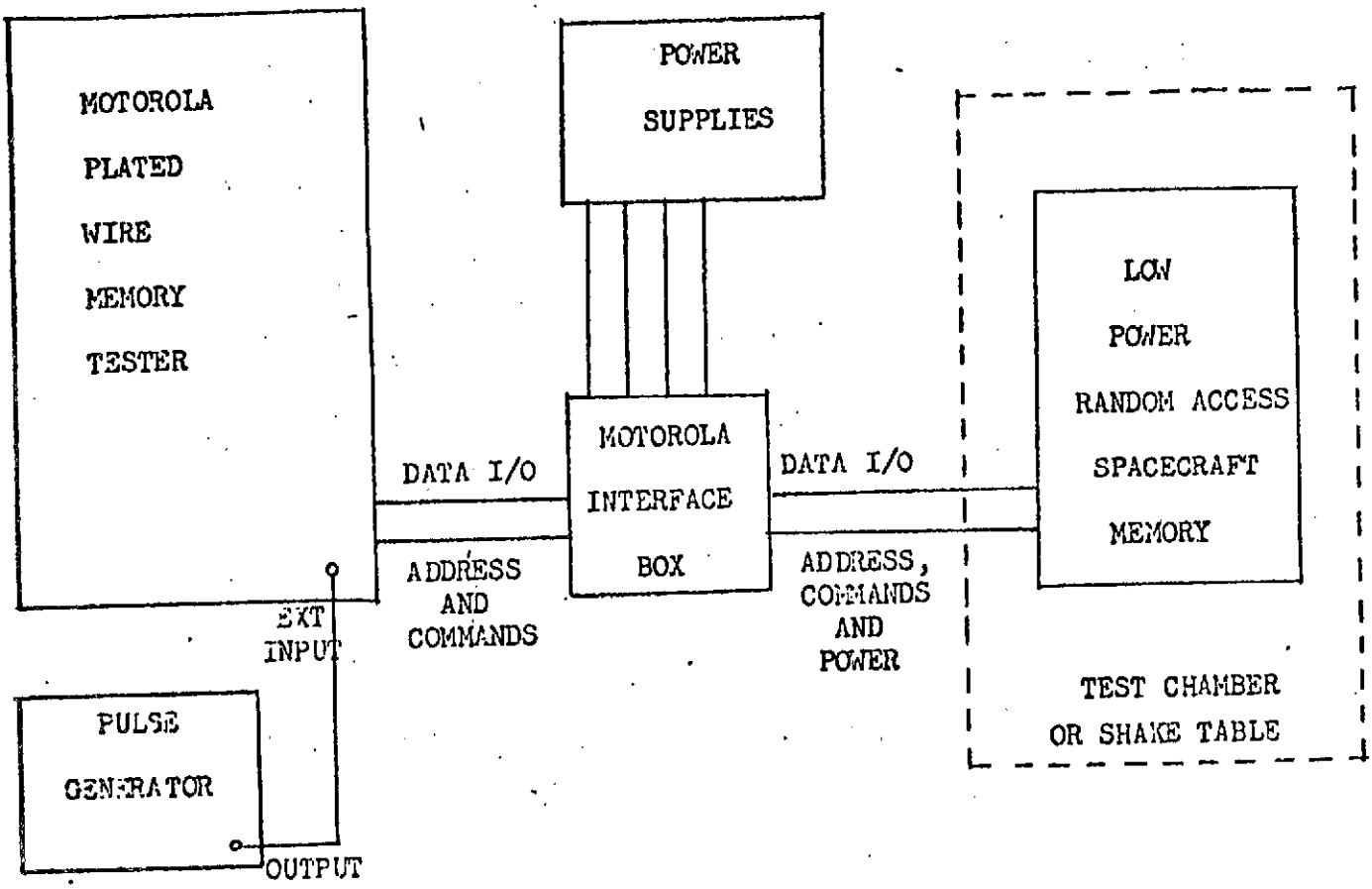


FIGURE 3. TEST SET UP

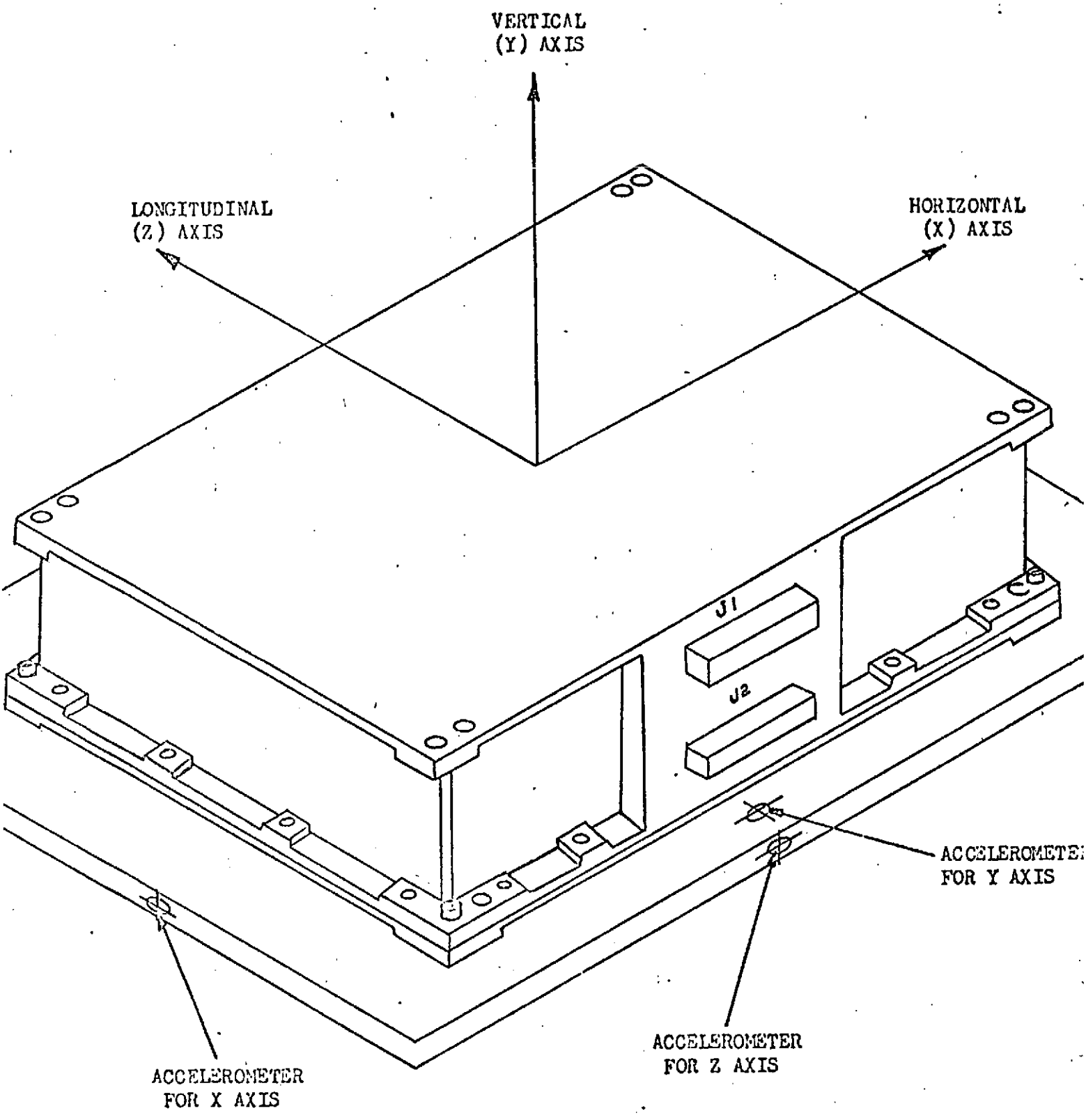
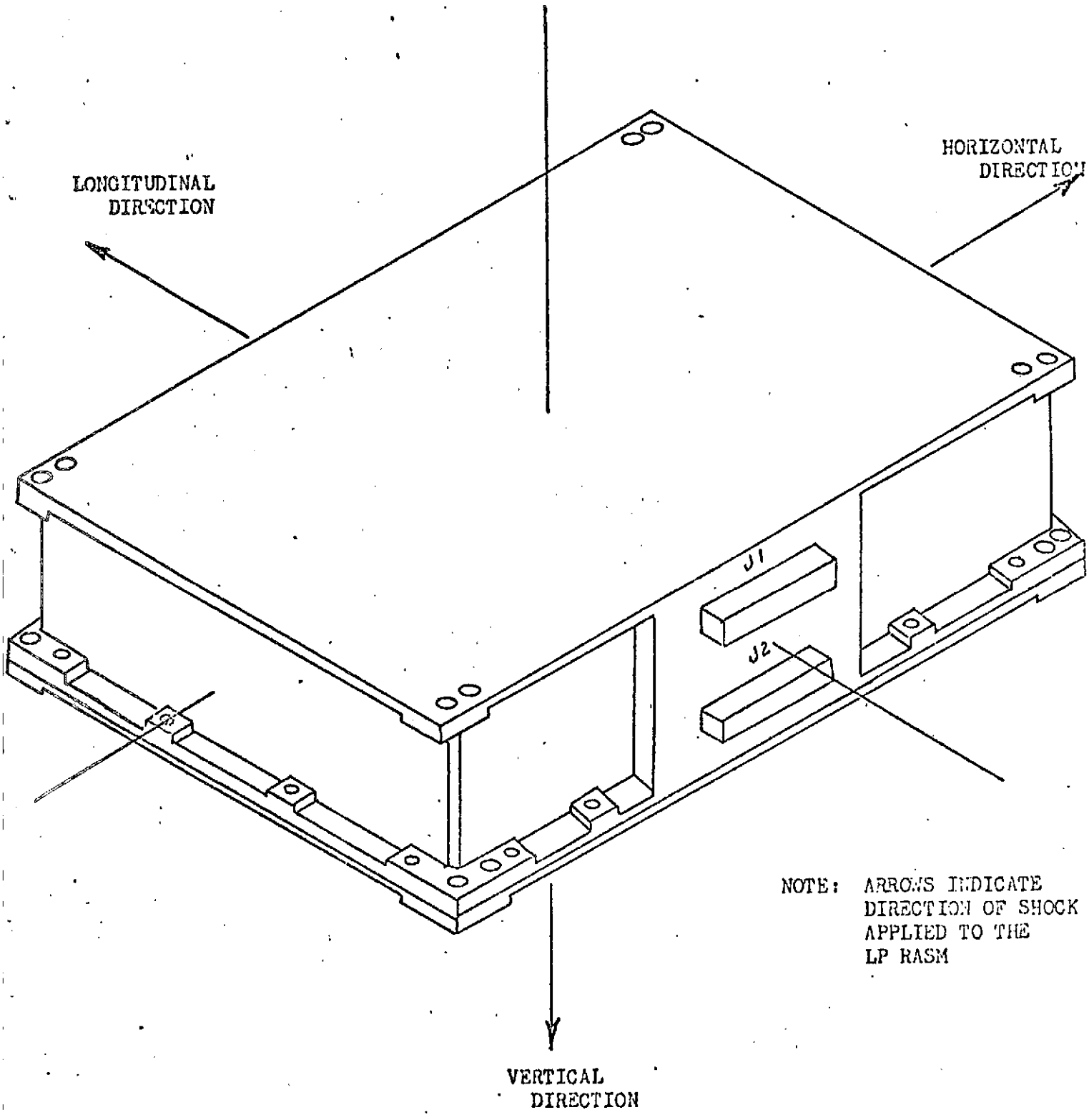


FIGURE 4. VIBRATION AXES

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13722D	72
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE NONE	REVISION		SHEET 34

V-2-8-1991-166A-3 69 DWG FORMAT



NOTE: ARROWS INDICATE DIRECTION OF SHOCK APPLIED TO THE LP RASM

FIGURE 5. SHOCK DIRECTIONS

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALL, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13722D	73
	SCALE NONE	REVISION		SHEET 35

APPLICATION

NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY - FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed

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REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																					
SHEET	27	28	29	30	31	32	33	34	35																					

REV STATUS OF SHEETS																															
REV	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X3	X4	X1	X4	X1	X1	X1	X1	X1	X1	X			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	2					

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339

CONTR NO. NAS 5-23163

RELEASE NOTICE

APPROVED 1-2-73 DATE

APPROVED DATE

MATERIAL:

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 101 Start Date of Tests 10-25-73

Tested by Ken Laquente MMC

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

COUNTER TSI 361-R
PULSE GEN. EH 138
HP 3442 PLUG-IN
DIGITEC 269 MULTIMETER
OVEN WALE 3600

4. PHYSICAL CHARACTERISTICS Limit

4.1 WEIGHT

Weight of LP-RASM = 6.25 Pounds 6.5 pounds (M 138)

S/N 101

Date of Test 10-25-73

Tested By MWC

6.2 DIMENSIONS

		Limit
H = 2.919 inches	(M 154)	
W = 8.632 inches	(M 154)	
MW = 9.971 inches	(M 154)	
D = 6.328 inches	(M 154)	
MD = 7.180 inches	(M 154)	
V = H X W X D = 159.45 inches^3	(M 154)	≤ 160 inches^3

(M NCR 69-1)

	SIZE	CODE IDENT NO.	DWG NO.	
Electronics Division	A	94990	12-P13721D	76
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION	SHEET 3	

DO NOT SCALE DRAWING

S/N 101 Date of Test 10-25-73

Tested By PMC

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	>10 MΩ	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	.609 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	1.1 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	.629 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	1.09 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	.671 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.58 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	.676 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	1.62 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	.633 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	1.12 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.761 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	2.06 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.921 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	.66 μa	≤ 20 μa

S/N [illegible] 101 Mine

Date of Test 10-25-73

Tested By Mine

		Limits
Current from ADDRESS 2^1 to Gnd	.923 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	.70 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.931 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	.68 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.931 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	.64 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.927 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	.63 μa	≤ 20 μa

Current from ADDRESS 2^5 to Gnd [illegible] ma

Current from ADDRESS 2^6 to Gnd [illegible] ma

Current from 2.4V to ADDRESS 2^5 [illegible]

Current from ADDRESS 2^7 to Gnd	.811 ma	
Current from 2.4V to ADDRESS 2^7	.86 μa	≤ 20 μa
Current from ADDRESS 2^8 to Gnd	.937 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.50 μa	≤ 20 μa
Current from ADDRESS 2^9 to Gnd	.897 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	.51 μa	≤ 20 μa
Current from ADDRESS 2^{10} to Gnd	.917 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	2.02 μa	≤ 20 μa
Current from ADDRESS 2^{11} to Gnd	.896 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	2.03 μa	≤ 20 μa
Current from DATA IN BIT 0 to Gnd	.972 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	.21 μa	≤ 20 μa

S/N 101

Date of Test 11-25-69

Tested By [illegible]

		Limits
Current from DATA IN BIT 1 to Gnd	.972 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	.23 μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	.984 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	.21 μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	.854 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	.93 μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	.858 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	1.01 μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	.841 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	1.01 μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	1.182 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	1.01 μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	1.122 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	.99 μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	1.193 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	1.03 μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	.843 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	.80 μa	≤ 20μa

S/N 101

Date of Test 10-25-72

Tested By [illegible]

		Limits
Current from DATA IN BIT 10 to Gnd	.834 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	.70 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.826 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	.68 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.839 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	.92 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.832 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	.80 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.839 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	.80 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.835 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	.90 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.832 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.89 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.832 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	~~.704~~ 1.04 μa	≤ 20μa

S/N 101

Date of Test 10-25-23

Tested By MAC

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	80 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	<80 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	<80 mv	≤ 100 mv

S/N 101

Date of Test 10-25-73

Tested By THC

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.003 Volts	
	Memory -6.1V voltage	-6.104 Volts	
	+5V Current	10.5 ma	
	+5V Power	52.5 mw	
7.7.2	Memory -6.1V Current	3.2 ma	
	Memory -6.1V Power	19.5 mw	
7.7.3	Total Memory Idle Power	72.0 mw	170 mw max
7.7.5	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V Voltage	-6.10 Volts	
	+5V Current	675 ma	
	+5V Power	3375 mw	
7.7.6	Memory -6.1V Current	165 ma	
	Memory -6.1V Power	1006.5 mw	
7.7.7	Total Active Power	4381.5 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	360 ns	500 ns max.
	Duration	300 ns	250 ns min 450 ns max.

A (1)

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 10

AV-2-B-199H-100A-3.69 DWG FORMAT

S/N 101

Date of Test 10-25-23

Tested by RWC

			LIMITS
7.8.7 & 7.8.8	READ COMPLETE/DATA OUTPUT TIMING		
	DO-0	OK X REJECT	
	DO-1	OK X REJECT	
	DO-2	OK X REJECT	
	DO-3	OK X REJECT	
	DO-4	OK X REJECT	
	DO-5	OK X REJECT	
	DO-6	OK X REJECT	
	DO-7	OK X REJECT	REFER TO TEST PROC.
	DO-8	OK X REJECT	
	DO-9	OK X REJECT	
	DO-10	OK X REJECT	
	DO-11	OK X REJECT	
	DO-12	OK X REJECT	
	DO-13	OK X REJECT	
	DO-14	OK X REJECT	
	DO-15	OK X REJECT	
	DO-16	OK X REJECT	
	DO-17	OK X REJECT	

A (M)

S/N 101

Date of Test 10-25-23
Tested By RHP

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur? No X Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur? No X Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur? No X Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur? No X Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur? No X Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur? a) No X Yes ____ Address ____ Bits ____	0 errors

S/N 101

Date of Test [illegible]
Tested By [illegible]

		Limits
	b) No X	
	Yes ____ Address ____ Bits ____	0 errors
	c) No X	
	Yes ____ Address ____ Bits ____	0 errors
7.11	NON-VOLATILITY TEST	
7.11.7 & 7.11.9	Did an error occur? No X	
	Yes ____ Address ____ Bits ____	0 errors
7.12	MEMORY SELECT TEST	
7.12.3	Address 0000 (Octal)	0000
7.12.4	Address 0001 0000 (Octal)	0000
	0010 0000 (Octal)	0000
	0011 0000 (Octal)	0000
	0100 0000 (Octal)	0000
	0101 0000 (Octal)	0000
	0110 0000 (Octal)	0000
	0111 0000 (Octal)	0000
	1000 0000 (Octal)	0000
	1001 0000 (Octal)	0000
	1010 0000 (Octal)	0000

A

S/N 101

Date of Test 10-25-73

Tested By Sue

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

S/N 101

Date of Test 10-25-73

Tested By KHC

Limits

7.13.4 a) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

b) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

S/N 101 Date of Test 10-25-73

Tested by JMC

8. TEMPERATURE TEST +85C at 10:45A Limits

8.2.1 Did any errors occur?

No X

Yes _____ Address _____ 0 Errors

Bits _____

8.2.3 Did any errors occur?

No X

Yes _____ Address _____ 0 Errors

Bits -- _____

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1,950 K ohms

60 minutes 1,809 K ohms % change 7.2

70 minutes 1,722 K ohms % change 4.8

80 minutes _____ K ohms % change _____

90 minutes _____ K ohms % change _____

8.2.5 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 5.0 ma +5V Current 11.6 ma

-6.1V Power 32 mw +5V Power 60.9 mv

Total Memory Idle Power 92.9 mw 170 mw max.

S/N 101 • Date of Test 10-25-23

Tested by JKC

8.2.6 Did an error occur? Limits

No X

Yes _____ Address _____ Bit _____ 0 errors

8.2.7 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 306 ma +5V Current 825 ma

-6.1V Power 1958.4 mw +5V Power 4331.3 mv

Total Memory Operate Power 6289.7 mw 7000 mw max.

8.2.8 WC a) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

S/N 101

DATE of TEST 10-25-73

Tested by BMC

		Limits
8.2.10	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.2.11	Did an error occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3	Low Temperature -40C at 1:35P	
8.3.3	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3.5	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	

S/N 101 Date of Test 10-25-73

Tested By TJC

8.3.6 LOW TEMPERATURE

Thermal Resistance

150 minutes 144.0 K ohms

160 minutes 148.4 K ohms % change 3.1

170 minutes _____ K ohms % change _____

180 minutes _____ K ohms % change _____

190 minutes _____ K ohms % change _____

8.3.7 Did an error occur? Limits

No X

Yes _____ Address _____ Bits _____ 0 Errors

8.3.8 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 10.9 ma +5V Current 11.0 ma

-6.1V Power 69.8 mw +5V Power 57.8 mw

Total Memory Idle Power 127.6 mw 170 mw max.

8.3.9 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 285 ma +5V Current 743 ma

-6.1V Power 1824 mw +5V Power 3900.8 mw

Total Memory Operate Power 5724.8 mw 7000 mw max.

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S/N 101 Date of Test 10-25-73

Tested By BHP

		Limits
8.3.10	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors
8.3.11	WC a) Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors
	WC b) Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors
	WC c) Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors
	WC d) Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors
8.3.13	Did any errors occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 Errors

A 93

7195

w.o. 1902

HIGH VACUUM TEST

Unit: Memory		Project: 3199	Date: 10/26/6
Model:		Specification: 1×10^{-5} & electrically
Serial:		Operator: Joe Mollere X
Vacuum System No.: 3		Observer: Ken Carpenter

TIME	PRESSURE (mm Hg A)	REMARKS
0930	ATM	
0935	1 MM	Go To Hi Vac
1030	2.5×10^{-5}	
1120	1.3×10^{-5}	
1215	8.7×10^{-6}	
1300	7.3×10^{-6}	
1330	6.5×10^{-6}	
1400	6×10^{-6}	
1430	5.3×10^{-6}	
1500	5×10^{-6}	
1530	4.6×10^{-6}	
1600	4.3×10^{-6}	
0845		Go To H. Vac
0920	1.3×10^{-5}	
1000	6.3×10^{-6}	
1035	3.9×10^{-6}	
1105	3.5×10^{-6}	94
1130	3×10^{-6}	
1215	2.7×10^{-6}	Vent To Atm.

S/N 101

Date of Test 10-26-73

Tested by RHC

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date 10-26-73 Tested by RHC

Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date 10-29-73 Tested by RHC

Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date 10-29-73 Tested by RHC

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No X

Yes _____ Freq _____ Address _____ Bits ____ 0 Errors

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MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 21

A-2-2-199H-100A-3/69 DWG FORMAT

MOTOROLA INC.
Government Electronics Division
Aerospace Center

VIBRATION TEST

Sheet 1 of 1 Date 29 Oct 73

Project 7195 Unit Random Access Memory

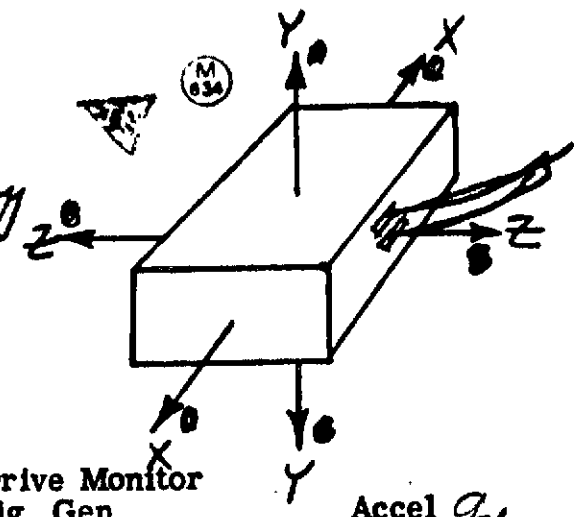
Serial No. 101

Operator E. SMITH / P. MARTIN

Observer KEN CARPENTER

Cycle Time _____ Freq. _____ to _____ cps.

Reason for test _____



Drive Monitor
Sig. Gen ____

Accel g

Axis	Time Start	Time Stop	Total Time		IN E DH	G RMS	Remarks
X	15:35	15:36	20 sec			5.64g	shaped random
X	15:40	15:41	20 sec			5.64g	"
X	15:49	15:50	20 sec			5.64g	" plot acc on case
X	16:23	16:25	2 min			5.64g	shaped random
X	1630	1634 ZY	4 ZY		.33	10 F PK 5.0	5-2KHZ PLOT 9
Z	1650	1654 ZY	4 ZY		.33	10 F PK 5.0	" PLOT 9
Z	1705	1707	2 MIN.		—	5.64 RMS	SHAPED RANDOM NOISE
Y	1917	1919	2 MIN			5.64 RMS	" " "
Y	1923	1927 ZY	4 ZY		.33	10 F 5.0	5-2KHZ

PROJECT 7195 UNIT 01-P13701D001 SER. NO. 101

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5HZ SCAN RATE 1.25HZ AVG. TIME 10 SECONDS
2. 10HZ SCAN RATE 2.25HZ AVG. TIME 10 SECONDS
3. 20HZ SCAN RATE 3.5 HZ AVG TIME 10 SECONDS
4. 50HZ SCAN RATE 41.25 AVG TIME 10 SECONDS

FREQ. RANGE 1. 15-20HZ MOTOROLA
20-40
40-100
100-2K

10/29/73

10/29/73

N-A

Response accel. (in-axis) top of unit

8.3

97

PROJECT 7195 UNIT 01-P13701D001 SER. NO. 101

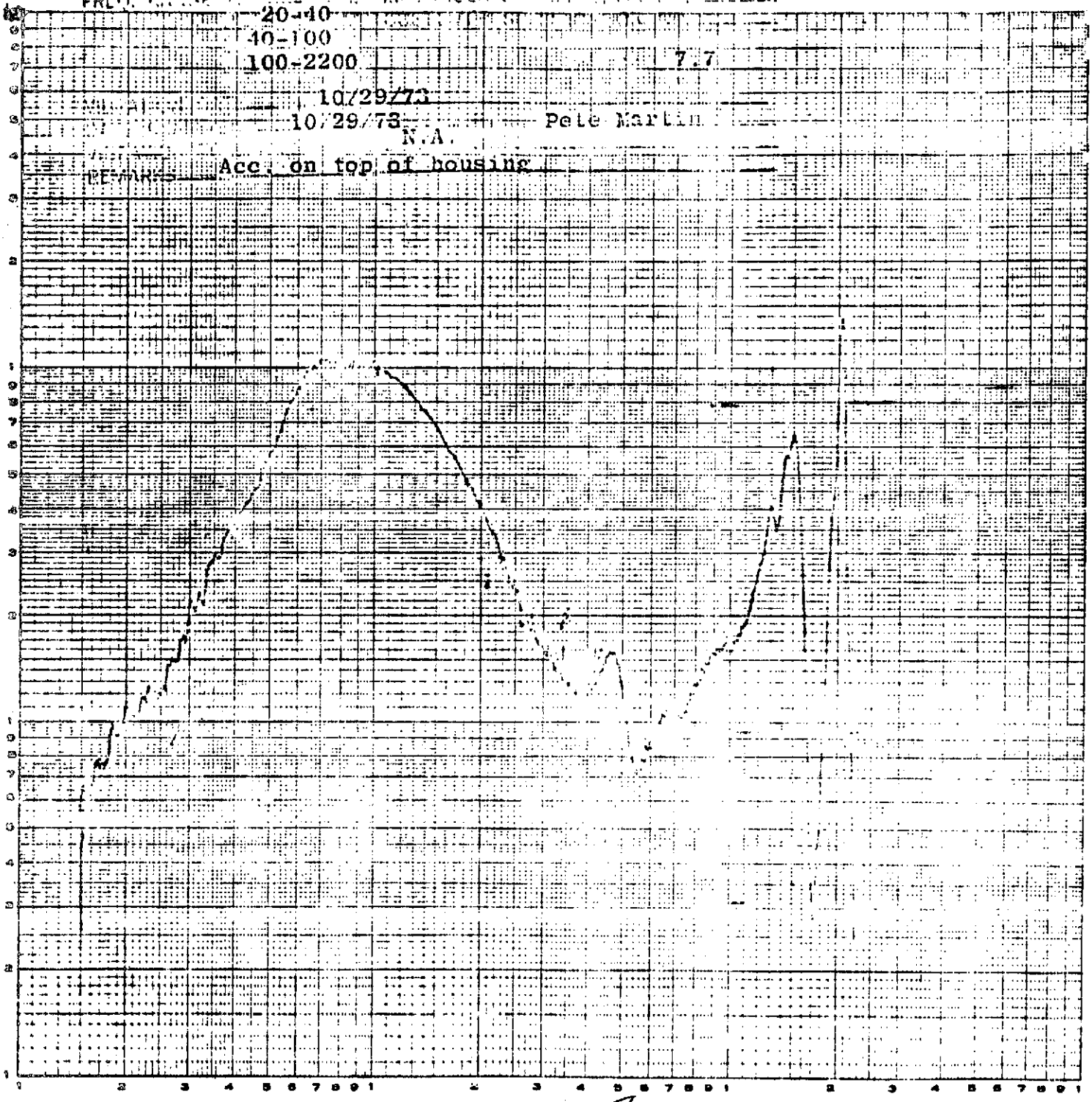
X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1.10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 1.10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG TIME 1.10 SECONDS
4. 50 HZ SCAN RATE 11.25 AVG TIME 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA LOCATION N.A.
2. 20-40
3. 40-100
4. 100-2200 7.7

10/29/73
10/29/73 Pete Martin
N.A.

REMARKS Acc. on top of housing



EUGENE DIETZGEN CO. MADE IN U.S.A.

98

PROJECT 7195 UNIT 01P13701D001 SER. NO. 101

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

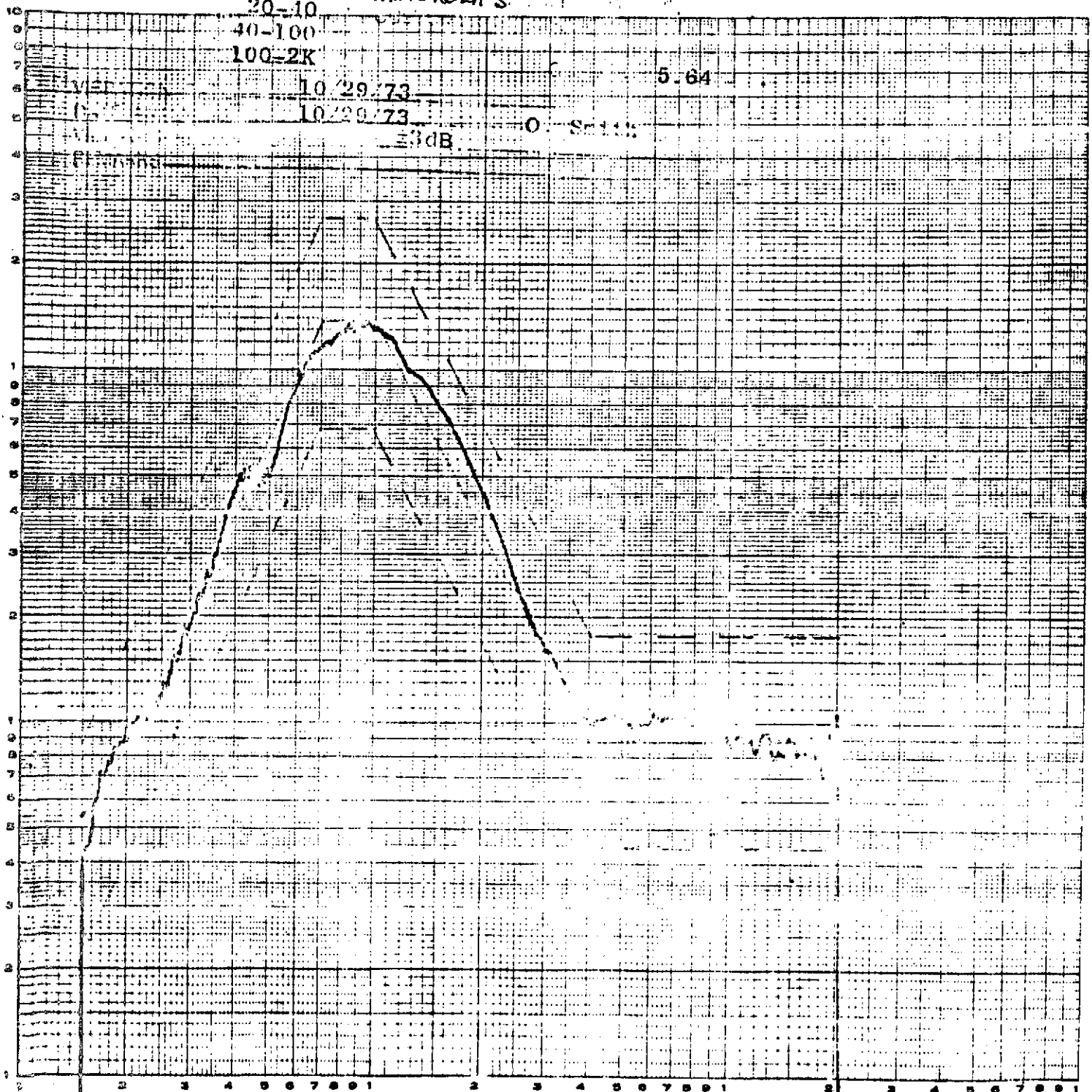
FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 10. SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 10. SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG TIME 10. SECONDS
4. 50 HZ SCAN RATE 1.25 HZ AVG TIME 10. SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA S[illegible]
20-40
40-100
100-2K

10/29/73
10/29/73

5.64

-3dB



99

PROJECT 7195 UNIT 01-P13701D001 SER. NO. 101

X & Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1: 125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. 25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. 5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4. 25 HZ AVG. TIME 4. 10 SECONDS

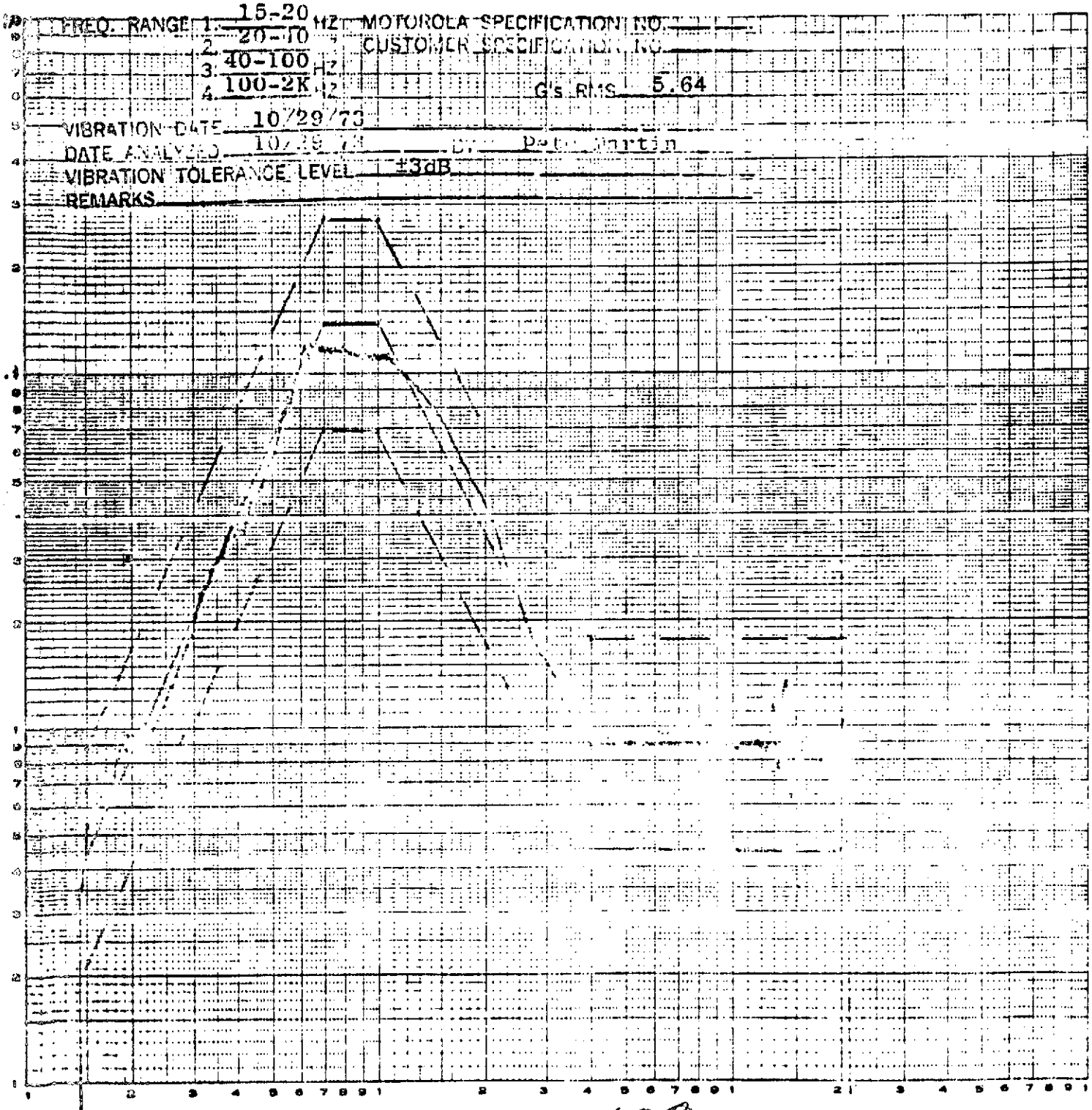
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ G's RMS 5.64

VIBRATION DATE 10/29/73

DATE ANALYZED 10/29/73 BY Pete Martin

VIBRATION TOLERANCE LEVEL ±3dB

REMARKS



100

SHOCK TEST
(DROP)

Sheet 1 of 1912 Date 11-2-73

Project 7195

Unit PWM

Operator Lee H

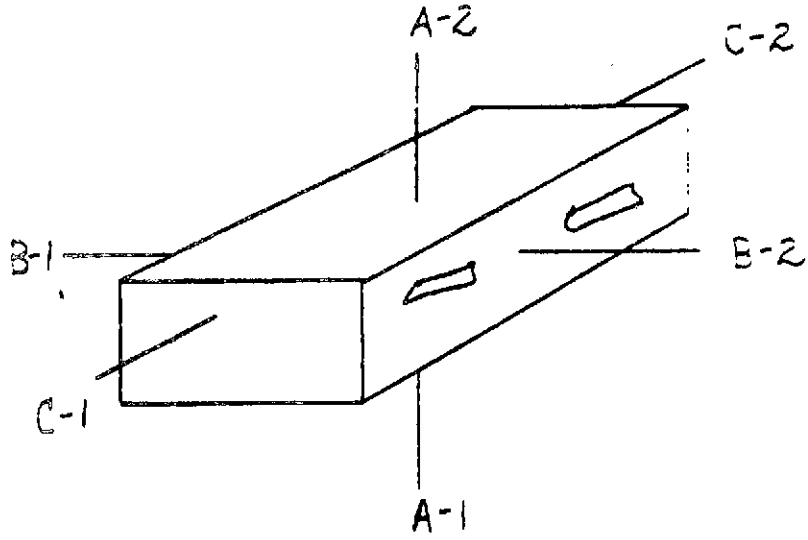
Observer Ken Carpenter

Vibration Mounts Lisa

No. of drops on each Axis 2 Total of 6

Acceleration 30 g ½ sine

Duration 6 (12) Milliseconds ±10%



Axis	Face	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
		6 ms					12 ms														
A	1	1	1				1														
	2																				
B	1			0				1													
	2																				
C	1																				
	2				1				1												

Remarks 6 ms 1 in L = 1", 1 in ½ cal open 25 ft tons ft

12 ms 1 in L = 3½", 1 in 1" thru closed, 1 in 1" thru open 1 in ½ cal open

+25 dB Wrms Lisa 101

BNF @ 0.2 g 4300 Hz

MN 102

Date of Test 10-29-73

Tested by KHR

Axis Y - Did Any Bit Error Occur? **Limits**

No X

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No X

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No X

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No X

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No X

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

11. SHOCK TEST

Date 11-2-73 Tested By KHR

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

S/N 101

Date of Test 11-2-73

Tested by RJC

Limits

Z Direction - Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

S/N 101 Date of Test 11-2-73

Tested By BHC

		Limit
7.4	CHASSIS ISOLATION	
	Impedance >10 MΩ	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.092 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 1.19 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd 1.088 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 .86 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd 1.092 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 1.16 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd 1.092 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 1.22 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd 1.089 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 .87 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd .743 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 2.11 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd .923 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 .72 μa	≤ 20 μa

S/N 101

Date of Test 11-2-23

Tested By [illegible]

		Limits
Current from ADDRESS 2^1 to Gnd	.928 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	.75 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.932 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	.73 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.934 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	.68 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.921 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	.68 μa	≤ 20 μa

S/N 101

Date of Test 11-2-73

Tested By BMC

		Limits
Current from ADDRESS 2^5 to Gnd	.825 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	1.05 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.938 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.67 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.818 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	.91 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	.942 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.54 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.919 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	.55 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.920 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	2.15 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.922 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	2.11 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	.976 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	.24 μa	≤ 20μa

S/N 101

Date of Test 11-2-78

Tested By JMC

		Limits
Current from DATA IN BIT 1 to Gnd	.998 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	.26 μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	.995 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	.25 μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	.866 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	.99 μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	.862 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	1.08 μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	.850 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	1.07 μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	1.192 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	1.07 μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	1.230 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	1.05 μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	1.219 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	1.10 μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	.847 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	.85 μa	≤ 20μa

S/N 101

Date of Test 11-2-73

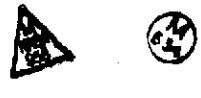
Tested By BJC

		Limits
Current from DATA IN BIT 10 to Gnd	.842 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	.25 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.830 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	.72 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.852 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	.97 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.838 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	.84 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.843 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	.85 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.838 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	.94 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.841 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.95 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.834 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	1.10 μa	≤ 20μa

S/N 101  Date of Test 11-2-73

Tested By MAE

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage 50	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage 60	mv	≤ 100 mv
	DATA OUT BIT 1 voltage 60	mv	≤ 100 mv
	DATA OUT BIT 2 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 3 voltage 100	mv	≤ 100 mv
	DATA OUT BIT 4 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 5 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 6 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 7 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 8 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 9 voltage 95	mv	≤ 100 mv
	DATA OUT BIT 10 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 11 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 12 voltage 80	mv	≤ 100 mv
	DATA OUT BIT 13 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 14 voltage 90	mv	≤ 100 mv
	DATA OUT BIT 15 voltage 95	mv	≤ 100 mv
	DATA OUT BIT 16 voltage 95	mv	≤ 100 mv
	DATA OUT BIT 17 voltage 100	mv	≤ 100 mv



S/N 101

Date of Test 11-2-73

Tested By WHC

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V voltage	-6.10 Volts	
	+5V Current	9.8 ma	
	+5V Power	49.0 mw	
7.7.2	Memory -6.1V Current	3.0 ma	
	Memory -6.1V Power	18.3 mw	
7.7.3	Total Memory Idle Power	67.3 mw	170 mw max
7.7.5	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V Voltage	-6.10 Volts	
	+5V Current	811 ma	
	+5V Power	4055 mw	
7.7.6	Memory -6.1V Current	300 ma	
	Memory -6.1V Power	1830 mw	
7.7.7	Total Active Power	5885 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	350 ns	500 ns max.
	Duration	275 ns	250 ns min 450 ns max.

S/N 101

Date of Test 11-2-73

Tested by MHC

		LIMITS
7.8.7 & 7.8.8	READ COMPLETE/DATA OUTPUT TIMING	
DO-0	OK ✓ REJECT	
DO-1	OK ✓ REJECT	
DO-2	OK ✓ REJECT	
DO-3	OK ✓ REJECT	
DO-4	OK ✓ REJECT	
DO-5	OK ✓ REJECT	
DO-6	OK ✓ REJECT	
DO-7	OK ✓ REJECT	REFER TO TEST PROC.
DO-8	OK ✓ REJECT	
DO-9	OK ✓ REJECT	
DO-10	OK ✓ REJECT	
DO-11	OK ✓ REJECT	
DO-12	OK ✓ REJECT	
DO-13	OK ✓ REJECT	
DO-14	OK ✓ REJECT	
DO-15	OK ✓ REJECT	
DO-16	OK ✓ REJECT	
DO-17	OK ✓ REJECT	

S/N 101

Date of Test 11-2-73
Tested By DHE

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?

a) No X

Yes ___ Address ___ Bits ___ 0 errors

S/N 101

Date of Test 11-2-73
Tested By Mike

		Limits
b)	No X	
	Yes ____ Address ____ Bits ____	0 errors
c)	No X	
	Yes ____ Address ____ Bits ____	0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3	Address 0000 (Octal)	0000
7.12.4	Address 0001 0000 (Octal)	0000
	0010 0000 (Octal)	0000
	0011 0000 (Octal)	0000
	0100 0000 (Octal)	0000
	0101 0000 (Octal)	0000
	0110 0000 (Octal)	0000
	0111 0000 (Octal)	0000
	1000 0000 (Octal)	0000
	1001 0000 (Octal)	0000
	1010 0000 (Octal)	0000

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S/N 101

Date of Test 11-2-23

Tested By ZHC

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13721D

SCALE | REVISION | SHEET 34

S/N 101

Date of Test 11-2-23

Tested By [illegible]

Limits

7.13.4 a) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

b) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

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* APPLICATION	
EXT ASSEMBLY	USED ON

STERISK INDICATES DATA WHICH IS NONMANDATORY FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed

THIS DOCUMENT
CLEARED THROUGH
Q A RECORDS CENTER

EV	X1	X4	X1	X3	X1	X1	X1	X1	X1																				
EET	27	28	29	30	31	32	33	34	35																				
V STATUS	REV	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X3	X4	X1	X4	X1	X1	X1	X1	X1	X1	X1	X1
SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		

R ASSOCIATED LISTS SEE

ERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

LESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN NCHES AND END USE. FOR TOLERANCES SEE NOTE

TERIAL:

DR BY H. Tweed
CHK BY
MFG
PROJ NO. 4339
CONTR NO. NAS 5-23163
RELEASE NOTICE
APPROVED DATE 1-2-73 H. Tweed
APPROVED DATE

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET,
LOW POWER RANDOM ACCESS SPACE-
CRAFT MEMORY, DRAWING NO. 01-P13721D

SIZE	CONFIDENTIAL NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 101 Start Date of Tests 2-13-74

Tested by [illegible] 2123

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DIGITEC 269 DMM
TSI 361-R COUNTER
EH 138 PULSE GEN.

4. PHYSICAL CHARACTERISTICS Limit

6.1 WEIGHT

Weight of LP-RASM = N/A Pounds 6.5 pounds

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S/N _____ Date of Test _____

Tested By _____

6.2 DIMENSIONS

Limit

N/A

H = _____ inches

W = _____ inches

MW= _____ inches

D = _____ inches

MD= _____ inches

V = H X W X D = _____ inches^3 ≤ 160 inches^3

N/A

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MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 3

AV-2-199H-100A-3/69 DWG FORMAT

S/N 101 Date of Test 2-13-74

Tested By [illegible]

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	>10 MΩ	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd ____ ma	N/A	≤ 2 ma
	Current from 2.4V to INITIATE PULSE ____ μa		≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to MEM SEL 1 ____ μa		≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to MEM SEL 2 ____ μa		≤ 20 μa
	Current from MEM SEL 3 to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to MEL SEL 3 ____ μa		≤ 20 μa
	Current from MEM SEL 4 to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to MEM SEL 4 ____ μa		≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to READ/WRITE ____ μa		≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd ____ ma		≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 ____ μa	N/A	≤ 20 μa

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S/N 101

Date of Test 2-13-74

Tested By Gme

		Limits
Current from ADDRESS 2^1 to Gnd _____	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1 _____	μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd _____	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2 _____	μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd _____	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3 _____	μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd _____	ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4 _____	μa	≤ 20 μa

N/A

N/A

120

S/N 101

Date of Test 2-13-74

Tested By TAE

		Limits
Current from ADDRESS 2^5 to Gnd	N/A ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	____ μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	____ μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	____ μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	____ μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	____ μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	____ μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	____ μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	N/A μa	≤ 20μa

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S/N 101

Date of Test 2-13-74

Tested By THE

		Limits
Current from DATA IN BIT 1 to Gnd	N/A ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	N/A μa	≤ 20μa

122

S/N 101

Date of Test 2-13-74

Tested By TMC

		Limits
Current from DATA IN BIT 10 to Gnd	N/A ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	___ μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	___ μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	___ μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	___ μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	___ μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	___ μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	___ μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	___ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	N/A μa	≤ 20μa

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SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13721D

SCALE | REVISION | SHEET 8

S/N 101

Date of Test 2-13-74

Tested By [illegible]

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage N/A	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 1 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 2 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 3 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 4 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 5 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 6 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 7 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 8 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 9 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 10 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 11 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 12 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 13 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 14 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 15 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 16 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 17 voltage N/A	mv	≤ 100 mv

124

S/N 101

Date of Test 2-13-74

Tested By TMC

Limits

7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.00 Volts

Memory -6.1V voltage -6.10 Volts

+5V Current 8.9 ma

+5V Power TMC ~~3.5~~ 3.6 mw 44.5 mw

7.7.2 Memory -6.1V Current 3.6 ma

Memory -6.1V Power 21.9 mw

7.7.3 Total Memory Idle Power 66.4 mw 170 mw max

7.7.5 Memory +5V Voltage 5.00 Volts

Memory -6.1V Voltage -6.10 Volts

+5V Current 670 ma

+5V Power 3350 ~~250~~ mw TMC

7.7.6 Memory -6.1V Current 250 ma

Memory -6.1V Power 1525 mw

7.7.7 Total Active Power 4875 mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay N/A ns 500 ns max.

Duration N/A ns 250 ns min
450 ns max.

125

S/N 101

Date of Test 2-13-24

Tested by JHE

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK N/A	REJECT
DO-1	OK	REJECT
DO-2	OK	REJECT
DO-3	OK	REJECT
DO-4	OK	REJECT
DO-5	OK	REJECT
DO-6	OK	REJECT
DO-7	OK	REJECT
DO-8	OK	REJECT
DO-9	OK	REJECT
DO-10	OK	REJECT
DO-11	OK	REJECT
DO-12	OK	REJECT
DO-13	OK	REJECT
DO-14	OK	REJECT
DO-15	OK	REJECT
DO-16	OK	REJECT
DO-17	OK N/A	REJECT

REFER TO TEST PROC.

126

S/N 101

Date of Test 2-13-74
Tested By WHC

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No X

Yes ___ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?

a) No X

Yes ___ Address ___ Bits ___ 0 errors

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S/N 101

Date of Test 2-13-74
Tested By [illegible]

Limits

b) No X
Yes _____ Address _____ Bits _____ 0 errors

c) No X
Yes _____ Address _____ Bits _____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?
No X
Yes ____ Address _____ Bits _____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
0010 0000 (Octal) 0000
0011 0000 (Octal) 0000
0100 0000 (Octal) 0000
0101 0000 (Octal) 0000
0110 0000 (Octal) 0000
0111 0000 (Octal) 0000
1000 0000 (Octal) 0000
1001 0000 (Octal) 0000
1010 0000 (Octal) 0000

128

S/N 101

Date of Test 2-13-74

Tested By MHC

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0002 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.13.3 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

129

S/N 101

Date of Test 2-13-74

Tested By MHE

		Limits
7.13.4	a) Did an error occur? No X Yes _____ Address _____ Bit _____	0 errors
	b) Did an error occur? No X Yes _____ Address _____ Bit _____	0 errors

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S/N 101

Date of Test 2-13-74

Tested by JHE

8. **TEMPERATURE TEST** +85°C at 9:05A — **Limits**

8.2.1 Did any errors occur?

No X

Yes _____ Address _____ 0 Errors

Bits _____

8.2.3 Did any errors occur?

No X

Yes _____ Address _____ 0 Errors

Bits -- _____

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.755K ohms

60 minutes 1.615 K ohms % change 7.9

70 minutes 1.512 K ohms % change 6.3

80 minutes 1.454 K ohms % change 3.8

90 minutes _____ K ohms % change _____

8.2.5 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 5.2 ma +5V Current 10 ma

-6.1V Power 33.3 mw +5V Power 52.5 mv

Total Memory Idle Power 85.8 mw 170 mw max.

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MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
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Date of Test 2-13-74

Tested by MHC

8.2.6 Did an error occur? Limits

No X

Yes _____ Address _____ Bit _____ 0 errors

8.2.7 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 300 ma +5V Current 770 ma

-6.1V Power 1920 mw +5V Power 4043 mw

Total Memory Operate Power 5963 mw 7000 mw max.

8.2.8 WC a) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

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S/N 101

DATE of TEST 2-13-74

Tested by MHC

		Limits
8.2.10	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.2.11	Did an error occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3	Low Temperature -40°C at 12:25 P	
8.3.3	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3.5	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	

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S/N 101 Date of Test 2-13-74

Tested By [illegible]

8.3.6 LOW TEMPERATURE

Thermal Resistance

150 minutes 147.0 K ohms

160 minutes 150.1 K ohms % change 2.1

170 minutes _____ K ohms % change _____

180 minutes _____ K ohms % change _____

190 minutes _____ K ohms % change _____

8.3.7 Did an error occur? Limits

No X

Yes ____ Address _____ Bits _____ 0 Errors

8.3.8 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 10.5 ma +5V Current 9.3 ma

-6.1V Power 67.2 mv +5V Power 48.8 mv

Total Memory Idle Power 116 mv 170 mv max.

8.3.9 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 270 ma +5V Current 685 ma

-6.1V Power 1728 mw +5V Power 3596 mv

Total Memory Operate Power 5324 mw 7000 mw max.

134

S/N 101 Date of Test 2-13-74

Tested By YHE

8.3.10 Did an error occur? Limits

No X

Yes ____ Address ____ Bits ____ 0 Errors

8.3.11 WC a) Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

WC b) Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

WC c) Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

WC d) Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

8.3.13 Did any errors occur?

No X

Yes ____ Address ____ Bits ____ 0 Errors

135

S/N N/A

Date of Test _____

Tested by _____

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date _____ Tested by _____

Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date _____ Tested by _____

Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date _____ Tested by _____

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No _____

Yes _____ Freq _____ Address _____ Bits ____ 0 Errors

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S/N N/A Date of Test _____

Tested by _____

Axis Y - Did Any Bit Error Occur? Limits

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

11. SHOCK TEST

Date _____ Tested By _____

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

S/N N/A

Date of Test _____

Tested by _____

Limits

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

S/N N/A Date of Test _____

Tested By _____

		Limit
7.4	CHASSIS ISOLATION	
	Impedance _____	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE _____ μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 _____ μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 _____ μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 _____ μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 _____ μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to READ/WRITE _____ μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd _____ ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 _____ μa	≤ 20 μa

S/N N/A

Date of Test _____

Tested By _____

	Limits
Current from ADDRESS 2^1 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1 _____μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2 _____μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3 _____μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4 _____μa	≤ 20 μa

MOTOROLA INC.
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SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P137211

SCALE | REVISION | SHEET 25

S/N N/A

Date of Test _____

Tested By _____

		Limits
Current from ADDRESS 2^5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	_____ μa	≤ 20 μa
Current from ADDRESS 2^8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	_____ μa	≤ 20 μa
Current from ADDRESS 2^9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	_____ μa	≤ 20 μa
Current from ADDRESS 2^{10} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	_____ μa	≤ 20 μa
Current from ADDRESS 2^{11} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	_____ μa	≤ 20 μa
Current from DATA IN BIT 0 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	_____ μa	≤ 20 μa

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S/N N/A

Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 1 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	_____ μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	_____ μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	_____ μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	_____ μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	_____ μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	_____ μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	_____ μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	_____ μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	_____ μa	≤ 20μa

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S/N N/A

Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 10 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	_____ μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	_____ μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	_____ μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	_____ μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	____o____ μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	_____ μa	≤ 20μa

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S/N - N/A

Date of Test _____

Tested By _____

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage _____	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 1 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 2 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 3 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 4 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 5 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 6 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 7 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 8 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 9 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 10 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 11 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 12 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 13 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 14 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 15 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 16 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 17 voltage _____	mv	≤ 100 mv

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S/N N/A

Date of Test _____

Tested By _____

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage _____	Volts	
	Memory -6.1V voltage _____	Volts	
	+5V Current _____	ma	
	+5V Power _____	mw	
7.7.2	Memory -6.1V Current _____	ma	
	Memory -6.1V Power _____	mw	
7.7.3	Total Memory Idle Power _____	mw	170 mw max
7.7.5	Memory +5V Voltage _____	Volts	
	Memory -6.1V Voltage _____	Volts	
	+5V Current _____	ma	
	+5V Power _____	mw	
7.7.6	Memory -6.1V Current _____	ma	
	Memory -6.1V Power _____	mw	
7.7.7	Total Active Power _____	mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay _____	ns	500 ns max.
	Duration _____	ns	250 ns min 450 ns max.

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S/N N/A

Date of Test _____

Tested by _____

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK_____	REJECT_____
DO-1	OK_____	REJECT_____
DO-2	OK_____	REJECT_____
DO-3	OK_____	REJECT_____
DO-4	OK_____	REJECT_____
DO-5	OK_____	REJECT_____
DO-6	OK_____	REJECT_____
DO-7	OK_____	REJECT_____
DO-8	OK_____	REJECT_____
DO-9	OK_____	REJECT_____
DO-10	OK_____	REJECT_____
DO-11	OK_____	REJECT_____
DO-12	OK_____	REJECT_____
DO-13	OK_____	REJECT_____
DO-14	OK_____	REJECT_____
DO-15	OK_____	REJECT_____
DO-16	OK_____	REJECT_____
DO-17	OK_____	REJECT_____

REFER TO TEST PROC.

146

S/N N/A

Date of Test _____
Tested By _____

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No _____	
	Yes ____ Address _____ Bits _____	0 errors
7.9.4	Did an error occur?	
	No _____	
	Yes ____ Address _____ Bits _____	0 errors
7.9.10	Did an error occur?	
	No _____	
	Yes ____ Address _____ Bits _____	0 errors
7.9.16	Did an error occur?	
	No _____	
	Yes ____ Address _____ Bits _____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No _____	
	Yes _____ Address _____ Bits _____	0 errors
7.10.7	Did an error occur?	
	a) No ____	
	Yes ____ Address _____ Bits _____	0 errors

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S/N N/A

Date of Test _____
Tested By _____

		Limits
b)	No _____	
	Yes _____ Address _____ Bits _____	0 errors
c)	No _____	
	Yes _____ Address _____ Bits _____	0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3	Address _____ (Octal)	0000
7.12.4	Address 0001 _____ (Octal)	0000
	0010 _____ (Octal)	0000
	0011 _____ (Octal)	0000
	0100 _____ (Octal)	0000
	0101 _____ (Octal)	0000
	0110 _____ (Octal)	0000
	0111 _____ (Octal)	0000
	1000 _____ (Octal)	0000
	1001 _____ (Octal)	0000
	1010 _____ (Octal)	0000

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S/N N/A

Date of Test _____

Tested By _____

		Limits
Address 1011	_____ (Octal)	0000
1100	_____ (Octal)	0000
1101	_____ (Octal)	0000
1110	_____ (Octal)	0000

7.12.6 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

149

S/N N/A

Date of Test 2-13-24

Tested By [illegible]

		Limits
7.13.4	a) Did an error occur?	
	No _____	
	Yes _____ Address _____ Bit _____	0 errors
	b) Did an error occur?	
	No _____	
	Yes _____ Address _____ Bit _____	0 errors

150

# APPLICATION	
NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY – FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed

-151-

REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																					
SHEET	27	28	29	30	31	32	33	34	35																					
REV STATUS	REV	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X3	X4	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25				

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339

CONTR NO. NAS 5-23163

RELEASE NOTICE

APPROVED DATE

APPROVED DATE

MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 852

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY. PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 102 Start Date of Tests 8-25-73

Tested by R C Tao

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

HP 5265A DIGITAL VOLTMETER
HP 5245L ELECTRONIC COUNTER
DIGITEC 269 MULTIMETER

4. PHYSICAL CHARACTERISTICS Limit

6.1 WEIGHT

Weight of LP-RASM = 6.145 Pounds 6.5 pounds

152 7/26/73 RM

S/N 102

Date of Test 7-25-73

Tested By DOL

6.2 DIMENSIONS

		Limit
H =	2.890 inches	
W =	8.630 inches	
MW=	8.961 inches	
D =	6.318 inches	
MD=	7.174 inches	
V = H X W X D =	157.57 inches^3	≤ 160 inches^3

153 2T 7/25/73

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION	SHEET 3

RCC
7-30-73

S/N 102 Date of Test ~~7-25-73~~

Tested By RCC

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	>10	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.086 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	1.24 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.108 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	.65 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.114 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	.96 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.114 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	1.00 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.11 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	.69 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.757 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	1.43 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	1.06 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	.66 μa	≤ 20 μa

VOID - See SHEET 24

THIS SHEET N/A ROZ

154

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from ADDRESS 2^1 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	.65 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.07 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	.68 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	.64 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	.62 μa	≤ 20 μa

VOID - SEE SHEET 24
THIS SHEET N/A
RDZ

155

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from ADDRESS 2^5 to Gnd	.79 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.60 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.66 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.785 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	.56 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.034 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.51 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.999 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	.46 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.864 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.31 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.865 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.33 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	.84 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	.52 μa	≤ 20μa

VOID - SEE SHEET 26
THIS SHEET VOID
ROZ 5/6

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 1 to Gnd	.837 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	.62 μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	.83 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	.62 μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	.886 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	.52 μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	.809 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	.54 μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	.887 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	.56 μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	.958 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	.38 μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	.969 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	.38 μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	.930 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	.39 μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	.774 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	.86 μa	≤ 20μa

VOID -- SEE SHEET 27

THIS SHEET N/A RDZ 1/57

S/N _____ Date of Test 7-30-73

Tested By RGL

		Limits
Current from DATA IN BIT 10 to Gnd	.969 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	.78 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.963 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	.79 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.834 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	1.99 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.827 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	1.75 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.817 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	1.70 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.890 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	.55 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.885 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.55 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.890 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.52 μa	≤ 20μa

VOID - SEE SHEET 28

THIS SHEET a/d

KVZ

158

S/N _____

Date of Test 7-30-73

Tested By PGL

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	~~30~~ mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 1 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 2 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 3 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 4 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 5 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 6 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 7 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 8 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 9 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 10 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 11 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 12 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 13 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 14 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 15 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 16 voltage	_____ mv	≤ 100 mv
	DATA OUT BIT 17 voltage	_____ mv	≤ 100 mv

VOID - SEE SHEET 29

THIS SHEET N/A

REV 169

S/N 102

Date of Test 7-30-77

Tested By RGC

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V voltage	6.10 Volts	
	+5V Current	10.3 ma	
	+5V Power	515 mw	
7.7.2	Memory -6.1V Current	3.25 ma	
	Memory -6.1V Power	19.8 mw	
7.7.3	Total Memory Idle Power	713 mw	170 mw max
7.7.5	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V Voltage	6.10 Volts	
	+5V Current	RGC 638 ~~6.38~~ ma	
	+5V Power	RGC 3.5 ~~30.5~~ mw	
		RGC ~~100.5~~	
7.7.6	Memory -6.1V Current	~~100.05~~ ma	159 RGC
	Memory -6.1V Power	~~20.2~~ mw	97 RGC
7.7.7	Total Active Power	100.5 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	340 ns	500 ns max.
	Duration	260 ns	250 ns min 450 ns max.

VOID - SEE SHEET 36

THIS SHEET REV A 160

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 10

S/N 102

Date of Test 7-30-73

Tested by RCC

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK ✓	REJECT
DO-1	OK ✓	REJECT
DO-2	OK ✓	REJECT
DO-3	OK ✓	REJECT
DO-4	OK ✓	REJECT
DO-5	OK ✓	REJECT
DO-6	OK ✓	REJECT
DO-7	OK ✓	REJECT
DO-8	OK ✓	REJECT
DO-9	OK ✓	REJECT
DO-10	OK ✓	REJECT
DO-11	OK ✓	REJECT
DO-12	OK ✓	REJECT
DO-13	OK ✓	REJECT
DO-14	OK ✓	REJECT
DO-15	OK ✓	REJECT
DO-16	OK ✓	REJECT
DO-17	OK ✓	REJECT

REFER TO TEST PROC.

VO10 - SEE SHEET 31

THIS SHEET N/A

RFJ 1/6/

S/N 102

Date of Test 7-25-73
Tested By RJZ

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur? No ✓ Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur? No ✓ Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur? No ✓ Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur? No ✓ Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur? No ✓ Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur? a) No ✓ Yes ____ Address ____ Bits ____	0 errors

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S/N 102

Date of Test 7-23-73
Tested By [illegible]

Limits

b) No ✓
Yes ____ Address ____ Bits ____ 0 errors

c) No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
0010 0000 (Octal) 0000
0011 0000 (Octal) 0000
0100 0000 (Octal) 0000
0101 0000 (Octal) 0000
0110 0000 (Octal) 0000
0111 0000 (Octal) 0000
1000 0000 (Octal) 0000
1001 0000 (Octal) 0000
1010 0000 (Octal) 0000

163 RT 7/25/73

S/N 102

Date of Test 7-25-23

Tested By RPT

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

164

RT 7/25/23

S/N 102

Date of Test 7-25-

Tested By RDZ

Limits

7.13.4 a) Did an error occur?

No ✓

Yes _____ Address _____ Bit _____ 0 errors

b) Did an error occur?

No ✓

Yes _____ Address _____ Bit _____ 0 errors

165

S/N 102 Date of Test 7-27-73

Tested by BOJ

8.	TEMPERATURE TEST	Limits

8.2.1 Did any errors occur? NOTE! Reached +85°C @ 0829

No ✓

Yes _____ Address _____ 0 Errors

Bits _____

8.2.3 Did any errors occur?

No ✓

Yes _____ Address _____ 0 Errors

Bits _____

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.874 K ohms

60 minutes 1.730 K ohms % change 7.7

70 minutes 1.626 K ohms % change 6.0

80 minutes 1.556 K ohms % change 4.92

90 minutes _____ K ohms % change _____

8.2.5 -6.1V Voltage ~~-6.09~~ -6.39 LCB Volts +5V Voltage ~~5.00~~ 5.25 LCB Volts

-6.1V Current ~~3.95~~ 4.82 LCB ma +5V Current ~~110~~ 111.7 LCB ma

-6.1V Power 30.8 mw +5V Power 614 mv

Total Memory Idle Power 92.2 mw 170 mw max.

166

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION	SHEET 16

S/N 102

Date of Test 7-27-73

Tested by R.T.

		Limits
8.2.6	Did an error occur?	
	No ✓	
	Yes _____ Address _____ Bit _____	0 errors
8.2.7	-6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts	
	-6.1V Current 300 ma +5V Current 784 ma	
	-6.1V Power 1920 mw +5V Power 4116 mv	
	Total Memory Operate Power 6036 mw	7000 mw max.
8.2.8	WC a) Did an error occur?	
	No ✓	
	Yes _____ Address _____ Bits _____	0 Errors
	WC b) Did an error occur?	
	No ✓	
	Yes _____ Address _____ Bits _____	0 Errors
	WC c) Did an error occur?	
	No ✓	
	Yes _____ Address _____ Bits _____	0 Errors
	WC d) Did an error occur?	
	No ✓	
	Yes _____ Address _____ Bits _____	0 Errors

167

S/N 102 DATE of TEST 7-27-73

Tested by RJ

		Limits
8.2.10	Did any errors occur? (M #32) (M NASA) No ✓ Yes_____ Address_____ Bits_____	0 Errors
8.2.11	Did an error occur? (M #32) (M NASA) No ✓ Yes_____ Address_____ Bits_____	0 Errors
8.3 8.3.3	Low Temperature Did any errors occur? (M #32) chamber at -40°C @ 1041 7-27-73 (M NASA) No ✓ Yes_____ Address_____ Bits_____	0 Errors
8.3.5	Did any errors occur? (M #32) (M NASA) No ✓ Yes_____ Address_____ Bits_____	0 Errors

168

S/N 102 Date of Test 7-27-73

Tested By RDZ

8.3.6 LOW TEMPERATURE

Thermal Resistance

150 minutes 194.0 K ohms

160 minutes 218.0 K ohms % change 12.4

170 minutes 225.6 K ohms % change 3.5

180 minutes _____ K ohms % change _____

190 minutes _____ K ohms % change _____

8.3.7 Did an error occur? Limits

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

8.3.8 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 9.8 ma +5V Current 11.0 ma

-6.1V Power 62.72 mv +5V Power 57.75 mv

Total Memory Idle Power 120.47 mv 170 mv max.

8.3.9 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 262 ma +5V Current 683 ma

-6.1V Power 1677 mw +5V Power 3585 mv

Total Memory Operate Power 5262 mw 7000 mw max.

169

S/N 102 Date of Test 7-27-73

Tested By DJ

8.3.10 Did an error occur? 

No ✓

Yes _____ Address _____ Bits _____ Limits: 0 Errors

8.3.11 WC a) Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

8.3.13 Did any errors occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

170

W.O. 2021

HIGH VACUUM TEST

Unit P.W. MEMORY		Project 4339	Date 7-25-7
Model		Specification AFP 12-P8722D	
Serial 102		Operator JIM HAWKINS	
Vacuum System No.		Observer BOB LOTT	

TIME	PRESSURE (mm Hg A)											REMARKS
1550	ATM	AMB.										START PUMPING
1555	70μ											
1606	40μ											
1632	1.4×10^{-4}											
1700	8×10^{-5}											
1800	1.7×10^{-4}											
1900	8×10^{-5}											
2000	6×10^{-5}											
2100	5.5×10^{-5}											
2200	5×10^{-5}											
2300	4×10^{-5}											
0200	3×10^{-5}											
0300	2×10^{-5}											
0500	1.5×10^{-5}											
0600	1.3×10^{-5}											
0700	1×10^{-5}											
0900	4.2×10^{-6}	AMB										171
0930	7×10^{-6}	"										
1000	5.8×10^{-6}	"										
1030	5.5×10^{-6}	"										
1100	5.3×10^{-6}	"										

HIGH VACUUM TEST

W.O. 2021

Unit: P.W. MEMORY	Project: 439
Model:	Specification: HTP 12-P13722D
Serial: 102	Operator: JOE MOLLERE
Vacuum System No.:	Observer: BOB LETZ

Date: 4-26-73

TIME	PRESSURE (mm Hg A)											REMARKS
1130	4.9×10^{-6}		AMB									
1201	4.7×10^{-6}		"									
1230	4.5×10^{-6}		"									
130	4.5×10^{-6}		"									VENT TO ATM.

172

S/N 102

Date of Test 7-25-73

Tested by RDZ

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors RT 7/25/73

9.2.1 Fast Decompression

Date 7-25-73 Tested by RDZ

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors RT 7/25/73

9.2.2 Hard Vacuum

Date 7-26-73 Tested by RDZ

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date 7-26-73 Tested by RDZ

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No _____

Yes _____ Freq _____ Address _____ Bits _____ 0 Errors

173

MOTOROLA INC.
Government Electronics Division
Aerospace Center

VIBRATION TEST

Sheet 1 of ____ Date 26 July 73

Project 4339 Unit PW Memory

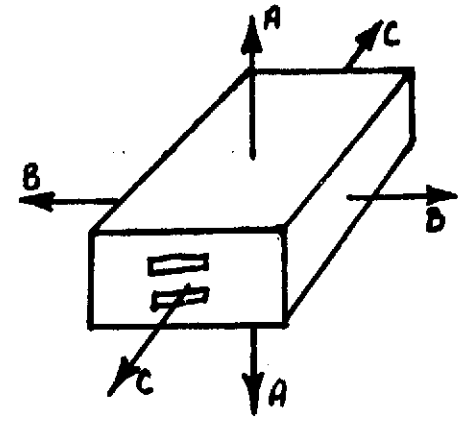
Serial No. 102

Operator Pete Martin

Observer Bob Lott

Cycle Time _____ Freq. _____ to _____ cps.

Reason for test _____



Drive Monitor
Sig. Gen ____

Accel g

Axis	Time Start	Time Stop	Total Time		E in DA	G pk	Remarks
A	15:38	15:42	4.3min		.33	10g+5g	sine sweep 5-110-2000 Hz
A	15:45	15:47	2min			5.64grms	shaped random
							174

S/N 102 Date of Test 7-26-73

Tested by RDZ

Axis Y - Did Any Bit Error Occur? Limits

No ✓

Yes ____ Freq _____ Address ____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ____

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No ____

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ____

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

11. SHOCK TEST

Date _____ Tested By _____

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ____

Yes ____ Address _____ Bits _____ 0 Errors

175

S/N_____ Date of Test_____

Tested by_____

Limits

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

176

S/N A102 Date of Test 7-30-73.

Tested By RGC

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	>10	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	.086 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	.24 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	.108 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	.65 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	.114 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	.96 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	.114 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	1.00 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	.11 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	.69 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.757 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	1.43 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	1.06 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	.66 μa	≤ 20 μa

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S/N 102

Date of Test 7-30-73

Tested By RGC

		Limits
Current from ADDRESS 2^1 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	.65 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.07 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	.68 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	.64 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	.62 μa	≤ 20 μa

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S/N 102 Date of Test 7-30-73

Tested By [illegible]

		Limits
Current from ADDRESS 2^5 to Gnd	.79 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.60 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	.66 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.785 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	.56 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.034 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.51 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.999 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	.46 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.864 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.31 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.865 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.33 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	.840 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	.52 μa	≤ 20μa

179

S/N 102

Date of Test 7-30-7[illegible]

Tested By RGC

		Limits
Current from DATA IN BIT 1 to Gnd	.837 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	.62 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	.830 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	.62 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	.886 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	.52 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	.809 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	.54 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	.887 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	.56 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	.958 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	.38 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	.969 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	.38 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	.930 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	.39 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.974 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	.86 μa	≤ 20 μa

180

S/N 102

Date of Test 7-30-73

Tested By KEC

		Limits
Current from DATA IN BIT 10 to Gnd	.969 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	.78 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.963 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	.79 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.834 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	1.99 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.827 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	1.75 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.817 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	1.70 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.890 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	.55 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.885 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.55 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.890 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	.52 μa	≤ 20μa

181

S/N 102

Date of Test 7-30-73

Tested By ROC

Limit

7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3	READ COMPLETE voltage	30	mv		≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	~~RC480~~	mv	95 RC83	≤ 100 mv
	DATA OUT BIT 1 voltage	~~RC480~~	mv	95 RC83	≤ 100 mv
	DATA OUT BIT 2 voltage	~~RC490~~	mv	90 RC83	≤ 100 mv
	DATA OUT BIT 3 voltage	~~RC440~~	mv	65 RC83	≤ 100 mv
	DATA OUT BIT 4 voltage	~~RC440~~	mv	60 RC83	≤ 100 mv
	DATA OUT BIT 5 voltage	~~RC440~~	mv	60 RC83	≤ 100 mv
	DATA OUT BIT 6 voltage	~~RC415~~	mv	95 RC83	≤ 100 mv
	DATA OUT BIT 7 voltage	~~RC440~~	mv	30 RC83	≤ 100 mv
	DATA OUT BIT 8 voltage	10	mv		≤ 100 mv
	DATA OUT BIT 9 voltage	95	mv		≤ 100 mv
	DATA OUT BIT 10 voltage	90	mv		≤ 100 mv
	DATA OUT BIT 11 voltage	90	mv		≤ 100 mv
	DATA OUT BIT 12 voltage	80	mv		≤ 100 mv
	DATA OUT BIT 13 voltage	75	mv		≤ 100 mv
	DATA OUT BIT 14 voltage	70	mv		≤ 100 mv
	DATA OUT BIT 15 voltage	80	mv		≤ 100 mv
	DATA OUT BIT 16 voltage	90	mv		≤ 100 mv
	DATA OUT BIT 17 voltage	95	mv		≤ 100 mv

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S/N .102

Date of Test 7-30-73

Tested By RGC

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V voltage	6.10 Volts	
	+5V Current	10.3 ma	
	+5V Power	51.5 mw	
7.7.2	Memory -6.1V Current	3.25 ma	
	Memory -6.1V Power	19.8 mw	
7.7.3	Total Memory Idle Power	71.3 mw	170 mw max
7.7.5	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V Voltage	6.10 Volts	
	+5V Current	638 ma	
	+5V Power	3.5 mw	
7.7.6	Memory -6.1V Current	159 ma	
	Memory -6.1V Power	97 mw	
7.7.7	Total Active Power	100.5 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	340 ns	500 ns max.
	Duration	260 ns	250 ns min 450 ns max.

183

S/N 102

Date of Test 2-30-73

Tested by RCC

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK ✓	REJECT
DO-1	OK ✓	REJECT
DO-2	OK ✓	REJECT
DO-3	OK ✓	REJECT
DO-4	OK ✓	REJECT
DO-5	OK ✓	REJECT
DO-6	OK ✓	REJECT
DO-7	OK ✓	REJECT
DO-8	OK ✓	REJECT
DO-9	OK ✓	REJECT
DO-10	OK ✓	REJECT
DO-11	OK ✓	REJECT
DO-12	OK ✓	REJECT
DO-13	OK ✓	REJECT
DO-14	OK ✓	REJECT
DO-15	OK ✓	REJECT
DO-16	OK ✓	REJECT
DO-17	OK ✓	REJECT

REFER TO TEST PROC.

184

S/N 102

Date of Test 7-30-73
Tested By Rec

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.9.4 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.9.10 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.9.16 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.10.7 Did an error occur?

a) No ✓

Yes ____ Address ____ Bits ____ 0 errors

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S/N 102

Date of Test 7-30-75
Tested By RLC

Limits

b) No ✓
Yes ____ Address ____ Bits ____ 0 errors

c) No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
0010 0000 (Octal) 0000
0011 0000 (Octal) 0000
0100 0000 (Octal) 0000
0101 0000 (Octal) 0000
0110 0000 (Octal) 0000
0111 0000 (Octal) 0000
1000 0000 (Octal) 0000
1001 0000 (Octal) 0000
1010 0000 (Octal) 0000

186

S/N 102

Date of Test 7-30-73

Tested By PGC

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

187

S/N 102

Date of Test 7-30-73

Tested By BLC

Limits

7.13.4 a) Did an error occur?

No ✓

Yes ____ Address ____ Bit ____ 0 errors

b) Did an error occur?

No ✓

Yes ____ Address ____ Bit ____ 0 errors

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* APPLICATION	
NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY – FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed

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REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																						
SHEET	27	28	29	30	31	32	33	34	35																						
REV STATUS OF SHEETS	REV	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X3	X4	X1	X4	X1	X1	X1	X1	X1	X1	X1	X1	X1
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26				

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND ENGINEER. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339

CONTR NO. NAS 5-23163

RELEASE DATE

APPROVED DATE 1-2-73 H. Tweed

APPROVED DATE

MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 102 Start Date of Tests 1-7-74

Tested by Ken Lapointe WNE

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DIGITEC 269 MULTIMETER
EH 138 PULSE GEN.
TSI 361-R COUNTER

4. PHYSICAL CHARACTERISTICS Limit

6.1 WEIGHT

Weight of LP-RASM = _____ Pounds 6.5 pounds

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Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	REV. A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 2

S/N _____ Date of Test _____

Tested By _____

6.2 DIMENSIONS

Limit

H = _____ inches

W = _____ inches

MW= _____ inches

D = _____ inches

MD= _____ inches

V = H X W X D = _____ inches^3 ≤ 160 inches^3

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MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 3

S/N 102 Date of Test 1-7-74

Tested By WHC

		Limit
7.4	CHASSIS ISOLATION	
	Impedance > 10 MΩ	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd _____ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE _____μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 _____μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 _____μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 _____μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 _____μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd _____ma	≤ 2 ma
	Current from 2.4V to READ/WRITE _____μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 _____μa	≤ 20 μa

192

S/N _____ Date of Test _____

Tested By _____

	Limits
Current from ADDRESS 2^1 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1 _____μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2 _____μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3 _____μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4 _____μa	≤ 20 μa

193

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from ADDRESS 2^5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	_____ μa	≤ 20 μa
Current from ADDRESS 2^8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	_____ μa	≤ 20 μa
Current from ADDRESS 2^9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	_____ μa	≤ 20 μa
Current from ADDRESS 2^{10} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	_____ μa	≤ 20 μa
Current from ADDRESS 2^{11} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	_____ μa	≤ 20 μa
Current from DATA IN BIT 0 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	_____ μa	≤ 20 μa

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S/N _____ Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 1 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	_____ μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	_____ μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	_____ μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	_____ μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	_____ μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	_____ μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	_____ μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	_____ μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	_____ μa	≤ 20 μa

195

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 10 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	_____ μa	≤ 20 μa
Current from DATA IN BIT 11 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	_____ μa	≤ 20 μa
Current from DATA IN BIT 12 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	_____ μa	≤ 20 μa
Current from DATA IN BIT 13 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20 μa
Current from DATA IN BIT 14 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20 μa
Current from DATA IN BIT 15 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	_____ μa	≤ 20 μa
Current from DATA IN BIT 16 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	_____ μa	≤ 20 μa
Current from DATA IN BIT 17 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	_____ μa	≤ 20 μa

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S/N ✓ Date of Test _____

Tested By _____

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage _____	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 1 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 2 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 3 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 4 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 5 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 6 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 7 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 8 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 9 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 10 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 11 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 12 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 13 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 14 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 15 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 16 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 17 voltage _____	mv	≤ 100 mv

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S/N 102

Date of Test 1-7-74

Tested By MHE

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V voltage	-6.10 Volts	
	+5V Current	10.4 ma	
	+5V Power	52 mw	
7.7.2	Memory -6.1V Current	3.3 ma	
	Memory -6.1V Power	20.1 mw	
7.7.3	Total Memory Idle Power	72.1 mw	170 mw max
7.7.5	Memory +5V Voltage	5.00 Volts	
	Memory -6.1V Voltage	-6.10 Volts	
	+5V Current	709 ma	
	+5V Power	3545 mw	
7.7.6	Memory -6.1V Current	268 ma	
	Memory -6.1V Power	1635 mw	
7.7.7	Total Active Power	5180 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	ns	500 ns max.
	Duration	ns	250 ns min 450 ns max.

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MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 10

AV-2-R-199H-100A-3 69 DWG FORMAT

S/N _____ Date of Test _____

Tested by _____

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK_____	REJECT_____
DO-1	OK_____	REJECT_____
DO-2	OK_____	REJECT_____
DO-3	OK_____	REJECT_____
DO-4	OK_____	REJECT_____
DO-5	OK_____	REJECT_____
DO-6	OK_____	REJECT_____
DO-7	OK_____	REJECT_____
DO-8	OK_____	REJECT_____
DO-9	OK_____	REJECT_____
DO-10	OK_____	REJECT_____
DO-11	OK_____	REJECT_____
DO-12	OK_____	REJECT_____
DO-13	OK_____	REJECT_____
DO-14	OK_____	REJECT_____
DO-15	OK_____	REJECT_____
DO-16	OK_____	REJECT_____
DO-17	OK_____	REJECT_____

REFER TO TEST PROC.

199

S/N 102

Date of Test 1-7-74
Tested By TAE

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.9.4 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.9.10 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.9.16 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.10.7 Did an error occur?

a) No X

Yes ____ Address ____ Bits ____ 0 errors

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S/N -102-

Date of Test 1-7-74
Tested By TME

		Limits
b)	No X	
	Yes ____ Address ____ Bits ____	0 errors
c)	No X	
	Yes ____ Address ____ Bits ____	0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?

No X

Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3	Address 0000 (Octal)	0000
7.12.4	Address 0001 0000 (Octal)	0000
	0010 0000 (Octal)	0000
	0011 0000 (Octal)	0000
	0100 0000 (Octal)	0000
	0101 0000 (Octal)	0000
	0110 0000 (Octal)	0000
	0111 0000 (Octal)	0000
	1000 0000 (Octal)	0000
	1001 0000 (Octal)	0000
	1010 0000 (Octal)	0000

201

S/N 102

Date of Test 1-7-24

Tested By [illegible]

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

202

S/N 102

Date of Test 1-7-74

Tested By BHC

Limits

7.13.4 a) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

b) Did an error occur?

No X

Yes ____ Address ____ Bit ____ 0 errors

S/N 102 Date of Test 1-7-74

Tested by HAC

8. TEMPERATURE TEST 1:15 PM +85C Limits

8.2.1 Did any errors occur?

No X X X X

Yes _____ Address _____ 0 Errors

Bits _____

8.2.3 Did any errors occur?

No X X X X

Yes _____ Address _____ 0 Errors

Bits --

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.707 K ohms

60 minutes 1.595 K ohms % change 6.6

70 minutes 1.515 K ohms % change 5.02

80 minutes 1.454 K ohms % change 4.02

90 minutes _____ K ohms % change _____

8.2.5 -6.1V Voltage -6.40 Volts +5V Voltage +5.25 Volts

-6.1V Current 5.0 ma +5V Current 11.7 ma

-6.1V Power 32 mw +5V Power 61.4 mv

Total Memory Idle Power 93.4 mw 170 mw max.

204

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 16

AV-2-B-199H-10CA-3 69 DSG FORMAT

S/N 102

Date of Test 1-7-74

Tested by XHC

8.2.6 Did an error occur? — Limits

No X

Yes _____ Address _____ Bit _____ — 0 errors

8.2.7 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 340 ma +5V Current 840 ma

-6.1V Power 2176 mw +5V Power 4410 mv

Total Memory Operate Power 6586 mw — 7000 mw max.

8.2.8 WC a) Did an error occur?

No X

Yes _____ Address _____ Bits _____ — 0 Errors

WC b) Did an error occur?

No X

Yes _____ Address _____ Bits _____ — 0 Errors

WC c) Did an error occur?

No X

Yes _____ Address _____ Bits _____ — 0 Errors

WC d) Did an error occur?

No X

Yes _____ Address _____ Bits _____ — 0 Errors

205

S/N 102

DATE of TEST 1-7-74

Tested by MHC

		Limits
8.2.10	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.2.11	Did an error occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3	Low Temperature 8:20A -40C	1-8-74
8.3.3	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	
8.3.5	Did any errors occur?	
	No X	
	Yes ____ Address ____	0 Errors
	Bits ____	

206

S/N 102 Date of Test 1-8-74

Tested By [illegible]

8.3.6 LOW TEMPERATURE

Thermal Resistance

150 minutes 145.2 K ohms

160 minutes 147.3 K ohms % change 1.4

170 minutes _____ K ohms % change _____

180 minutes _____ K ohms % change _____

190 minutes _____ K ohms % change _____

8.3.7 Did an error occur? Limits

No X

Yes _____ Address _____ Bits _____ 0 Errors

8.3.8 -6.1V Voltage -6.4 Volts +5V Voltage 5.25 Volts

-6.1V Current 9.3 ma +5V Current 11.2 ma

-6.1V Power 59.5 mv +5V Power 58.8 mv

Total Memory Idle Power 118.3 mv 170 mv max.

8.3.9 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 300 ma +5V Current 748 ma

-6.1V Power 1920 mw +5V Power 3927 mv

Total Memory Operate Power 5847 mw 7000 mw max.

207

S/N -102 Date of Test 1-8-74

Tested By Mike

8.3.10 Did an error occur? Limits

No X

Yes _____ Address _____ Bits _____ 0 Errors

8.3.11 WC a) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

8.3.13 Did any errors occur?

No X

Yes _____ Address _____ Bits _____ 0 Errors

208

S/N _____ Date of Test _____

Tested by _____

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date _____ Tested by _____

Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date _____ Tested by _____

Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date _____ Tested by _____

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No _____

Yes _____ Freq _____ Address _____ Bits ____ 0 Errors

209

S/N _____ Date of Test _____

Tested by _____

Axis Y - Did Any Bit Error Occur? Limits

No _____

Yes ____ Freq _____ Address ____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No _____

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

11. SHOCK TEST

Date _____ Tested By _____

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

210

S/N _____ Date of Test _____

Tested by _____

Limits

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No _____

Yes _____ Address _____ Bits _____ 0 Errors

211

S/N _____ Date of Test _____

Tested By _____

		Limit
7.4	CHASSIS ISOLATION	
	Impedance _____	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd _____ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE _____μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 _____μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 _____μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3_____μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 _____μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd _____ma	≤ 2 ma
	Current from 2.4V to READ/WRITE _____μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd _____ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0_____μa	≤ 20 μa

212

S/N _____ Date of Test _____

Tested By _____

	Limits
Current from ADDRESS 2^1 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1 _____μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2 _____μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3 _____μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd _____ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4 _____μa	≤ 20 μa

213

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from ADDRESS 2^5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	_____ μa	≤ 20 μa
Current from ADDRESS 2^7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	_____ μa	≤ 20 μa
Current from ADDRESS 2^8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	_____ μa	≤ 20 μa
Current from ADDRESS 2^9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	_____ μa	≤ 20 μa
Current from ADDRESS 2^{10} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	_____ μa	≤ 20 μa
Current from ADDRESS 2^{11} to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	_____ μa	≤ 20 μa
Current from DATA IN BIT 0 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	_____ μa	≤ 20 μa

214

S/N _____

Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 1 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	_____ μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	_____ μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	_____ μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	_____ μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	_____ μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	_____ μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	_____ μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	_____ μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	_____ μa	≤ 20 μa

215

S/N _____ Date of Test _____

Tested By _____

		Limits
Current from DATA IN BIT 10 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	_____ μa	≤ 20 μa
Current from DATA IN BIT 11 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	_____ μa	≤ 20 μa
Current from DATA IN BIT 12 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	_____ μa	≤ 20 μa
Current from DATA IN BIT 13 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20 μa
Current from DATA IN BIT 14 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	_____ μa	≤ 20 μa
Current from DATA IN BIT 15 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	_____ μa	≤ 20 μa
Current from DATA IN BIT 16 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	_____ μa	≤ 20 μa
Current from DATA IN BIT 17 to Gnd	_____ ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	_____ μa	≤ 20 μa

216

S/N _____

Date of Test _____

Tested By _____

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage _____	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 1 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 2 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 3 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 4 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 5 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 6 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 7 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 8 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 9 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 10 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 11 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 12 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 13 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 14 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 15 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 16 voltage _____	mv	≤ 100 mv
	DATA OUT BIT 17 voltage _____	mv	≤ 100 mv

217

S/N _____ Date of Test _____

Tested By _____

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage _____	Volts	
	Memory -6.1V voltage _____	Volts	
	+5V Current _____	ma	
	+5V Power _____	mw	
7.7.2	Memory -6.1V Current _____	ma	
	Memory -6.1V Power _____	mw	
7.7.3	Total Memory Idle Power _____	mw	170 mw max
7.7.5	Memory +5V Voltage _____	Volts	
	Memory -6.1V Voltage _____	Volts	
	+5V Current _____	ma	
	+5V Power _____	mw	
7.7.6	Memory -6.1V Current _____	ma	
	Memory -6.1V Power _____	mw	
7.7.7	Total Active Power _____	mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay _____	ns	500 ns max.
	Duration _____	ns	250 ns min 450 ns max.

218

S/N _____ Date of Test _____

Tested by _____

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK_____	REJECT_____
DO-1	OK_____	REJECT_____
DO-2	OK_____	REJECT_____
DO-3	OK_____	REJECT_____
DO-4	OK_____	REJECT_____
DO-5	OK_____	REJECT_____
DO-6	OK_____	REJECT_____
DO-7	OK_____	REJECT_____
DO-8	OK_____	REJECT_____
DO-9	OK_____	REJECT_____
DO-10	OK_____	REJECT_____
DO-11	OK_____	REJECT_____
DO-12	OK_____	REJECT_____
DO-13	OK_____	REJECT_____
DO-14	OK_____	REJECT_____
DO-15	OK_____	REJECT_____
DO-16	OK_____	REJECT_____
DO-17	OK_____	REJECT_____

REFER TO TEST PROC.

219

S/N _____ Date of Test _____

Tested By _____

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.9.4 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.9.10 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.9.16 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.10.7 Did an error occur?

a) No _____

Yes _____ Address _____ Bits _____ 0 errors

220

S/N _____ Date of Test _____

Tested By _____

		Limit
	b) No _____	
	Yes _____ Address _____ Bits _____	0 error
	c) No _____	
	Yes _____ Address _____ Bits _____	0 error
7.11	NON-VOLATILITY TEST	
7.11.7 & 7.11.9	Did an error occur?	
	No _____	
	Yes _____ Address _____ Bits _____	0 error
7.12	MEMORY SELECT TEST	
7.12.3	Address _____ (Octal)	0000
7.12.4	Address 0001 _____ (Octal)	0000
	0010 _____ (Octal)	0000
	0011 _____ (Octal)	0000
	0100 _____ (Octal)	0000
	0101 _____ (Octal)	0000
	0110 _____ (Octal)	0000
	0111 _____ (Octal)	0000
	1000 _____ (Octal)	0000
	1001 _____ (Octal)	0000
	1010 _____ (Octal)	0000

S/N _____ Date of Test _____

Tested By _____

		Limits
Address 1011 _____ (Octal)		0000
1100 _____ (Octal)		0000
1101 _____ (Octal)		0000
1110 _____ (Octal)		0000

7.12.6 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No _____

Yes _____ Address _____ Bits _____ 0 errors

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S/N _____ Date of Test _____

Tested By _____

Limits

7.13.4 a) Did an error occur?

No _____

Yes _____ Address _____ Bit _____ 0 errors

b) Did an error occur?

No _____

Yes _____ Address _____ Bit _____ 0 errors

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APPENDIX II

STACK TEST PROCEDURE

224

* APPLICATION	
NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY – FOR INFORMATION ONLY.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

225

REV																															
SHEET																															
REV STATUS OF SHEETS	REV																														
	SHEET																														

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY R. Bryant

CHK BY

MFG | PROJ NO. 4339

CONTR NO.

RELEASE NOTICE

APPROVED H. Tennent DATE 3-2-73

APPROVED DATE

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 8525

ACCEPTANCE TEST PROCEDURE FOR PLATED WIRE MEMORY STACK 4K x 18 (1024 WORD LINES, 72 DIGIT LINES)

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13729D

SCALE

1. SCOPE

1.1 This test procedure specifies the electrical tests to be performed on all 01-P13707D plated wire memory stacks.

2. APPLICABLE DOCUMENTS

2.1 Drawing No. 69-P07708E, Interconnect Drawing

2.2 Drawing No. 69-P13705D, Interconnect Diagram, Memory

2.3 Drawing No. 01-P13707D, Memory Stack Assembly

2.4 Drawing No. 69-P10930D, Diagram of the Word Drive Test Adapter Boxes.

2.5 Drawing N . 99-P07707E, Restore Timing.

3. SPECIAL REQUIREMENTS

3.1 Test cables as shown in Figures 1, 2, & 3.

3.2 Stack & Timing Interface Adapters 69-P10930D.

3.3 Four 52 pin to 64 pin adapters, 84-P04070D001.

4. STACK TESTER/ADAPTER BOX/STACK INTERCONNECT

4.1 The interconnections between the EH8500 Stack Tester, the Word Drive Test Adpater Box and the Word Line Interface Boards are shown in Interconnect Drawing No. 69-P07708E. Switches 1-5 are to be set to 4278, switches 6 & 7 to ON. The Sense & Word Line Interconnections are shown in Figures 4 & 5.

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5. TEST CONDITIONS

5.1 SENSE TERMINATION

The sense lines are to be terminated by 100 ohm (± 1%) resistors to ground. The terminating resistors may be mounted at the input to the sense amplifier.

5.2 STACK RESTORE

The Restore Timing is shown in the Restore Timing Drawing No. 99-P07707E. The restore pulse width is adjusted, along with the restore voltage, to recharge the previously selected first and second level word select lines to +5V at the beginning of the following cycle.

5.3 CURRENT PULSE WAVEFORMS

The current pulse waveforms (as shown in Figure 6) are to be set up initially using a current probe (calibrated to ± 1% @ 40 and 500 ma) to monitor the word and digit currents at the locations shown in Figure 7. The amplitudes of all currents are given in Section 5.4.

5.3.1 The overshoot on any current shall be less than 2% of the specified current amplitude.

5.3.2 The droop on any current shall be less than 2% of the specified current amplitude.

5.3.3 The overlap and steering for the word and digit currents is specified in Figure 6.

5.3.4 All times specified are ± 2%, or one nanosecond, whichever is greater.

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5.4 CURRENT AMPLITUDES

Current amplitudes are milliamperes, ± 1%, as measured at mid-point of the flat top.

5.4.1 Read Current

Read Current = I_{WR} = 475 ma.

5.4.2 Write Currents

Word Current = I_{WW} = 475 ma.

	$+25^{\circ}C \pm 5$	$95^{\circ}C$ $^{+5}_{-0}$	$-40^{\circ}C$ $^{+0}_{-5}$
Digit Current I_{DW1}	41.0	35.0	48.0
Digit Current I_{DW2}	39.0	33.0	46.0

5.4.3 Disturb Currents

Word Current = I_{WD} = 525 ma.

	$+25^{\circ}C \pm 5$	$95^{\circ}C$ $^{+5}_{-0}$	$-40^{\circ}C$ $^{+0}_{-5}$
Digit Current I_{DD1}	45.5	40.0	53.5
Digit Current I_{DD2}	48.0	42.0	57.0

5.5 TEMPERATURE TESTING

All electrical tests shall be performed at the three temperatures. The tests shall be run in the following order.

5.5.1 Test all outputs at 25 ± 5°C. Peak amplitude of output shall be 4.5 millivolts minimum.

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5.5.2 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.3 Repeat paragraph 5.5.1.

5.5.4 Test all outputs at 95 $^{+5}_{-0}$°C. Peak amplitude of all outputs shall be 4.5 millivolts minimum.

5.5.5 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.6 Repeat paragraph 5.5.4.

5.5.7 Test all outputs at -40 $^{+0}_{-5}$°C. Peak amplitude of all outputs shall be 4.5 millivolts minimum,

5.5.8 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.9 Repeat paragraph 5.5.7.

5.6 TEST PATTERN

The test pattern shall be as shown in Figure 8.

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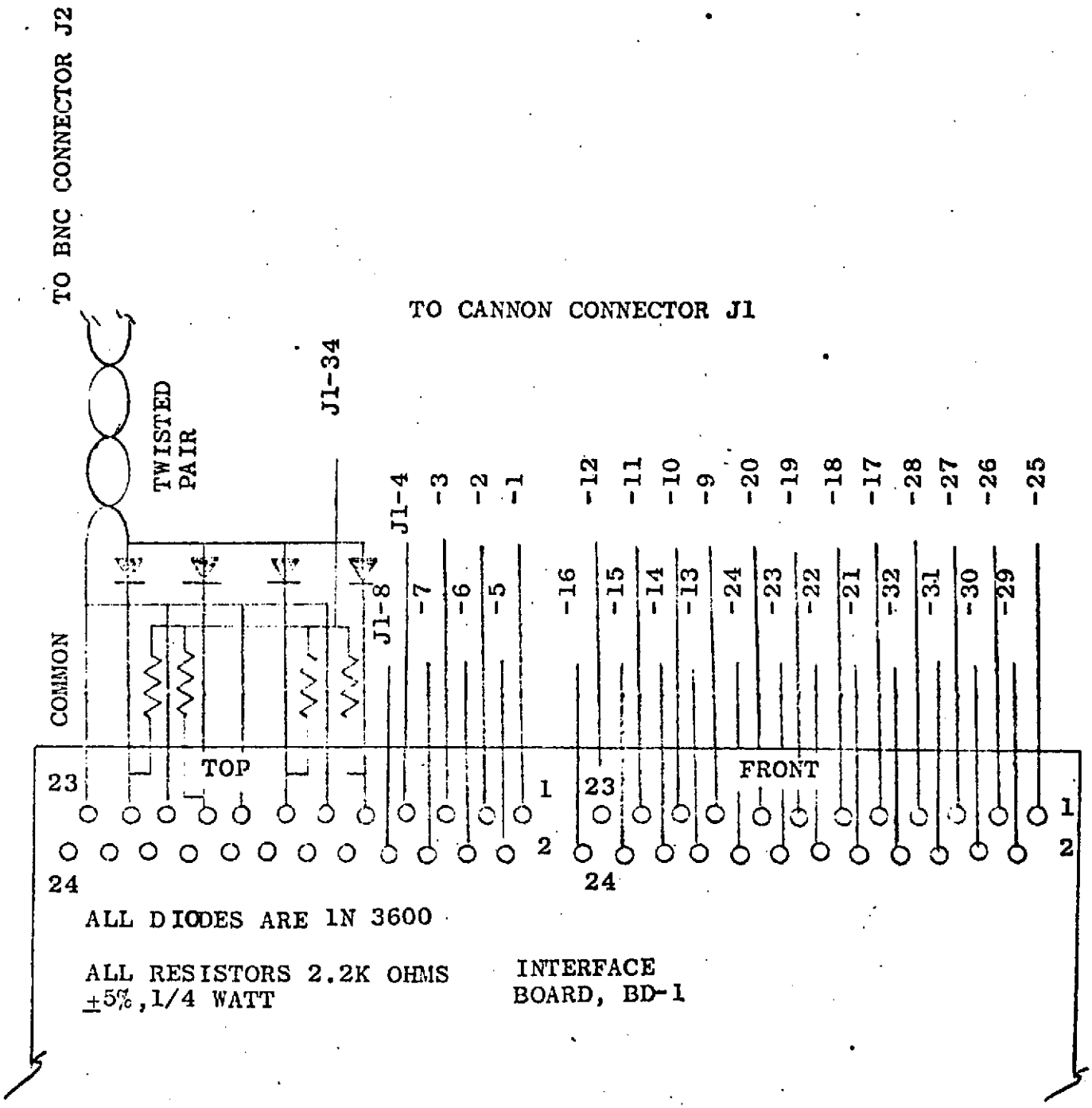

FIGURE 1: STACK TEST CABLE

230

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13729D
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION	SHEET 6
7-2-8-199H-100A-3.69 DWG FORMAT			

TO CANNON CONNECTOR J1

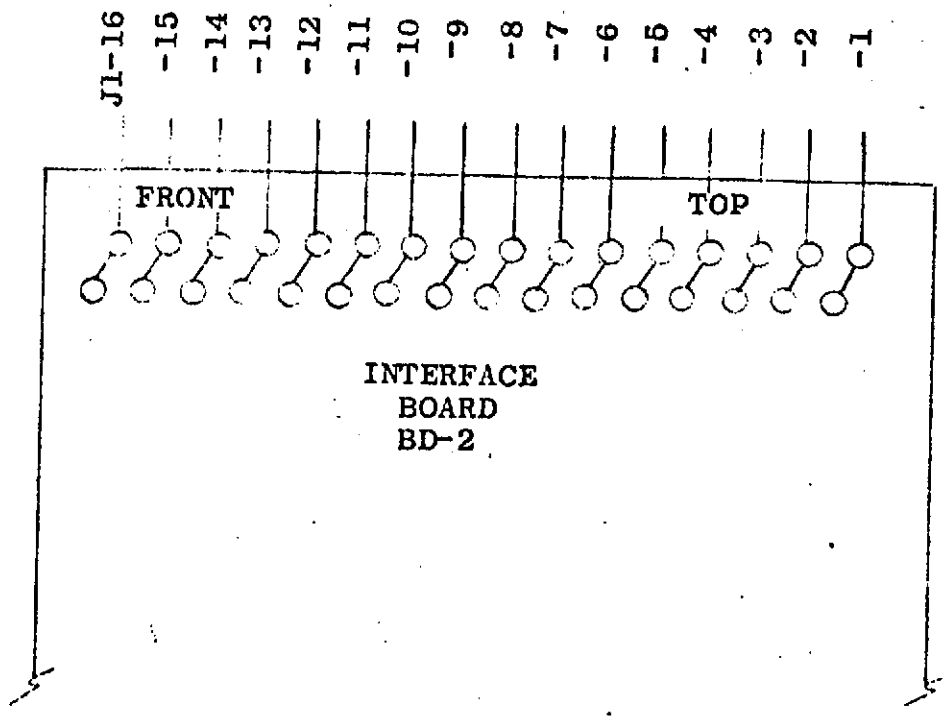

FIGURE 2: STACK TEST CABLE

231

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13729D
	SCALE	REVISION	SHEET 7

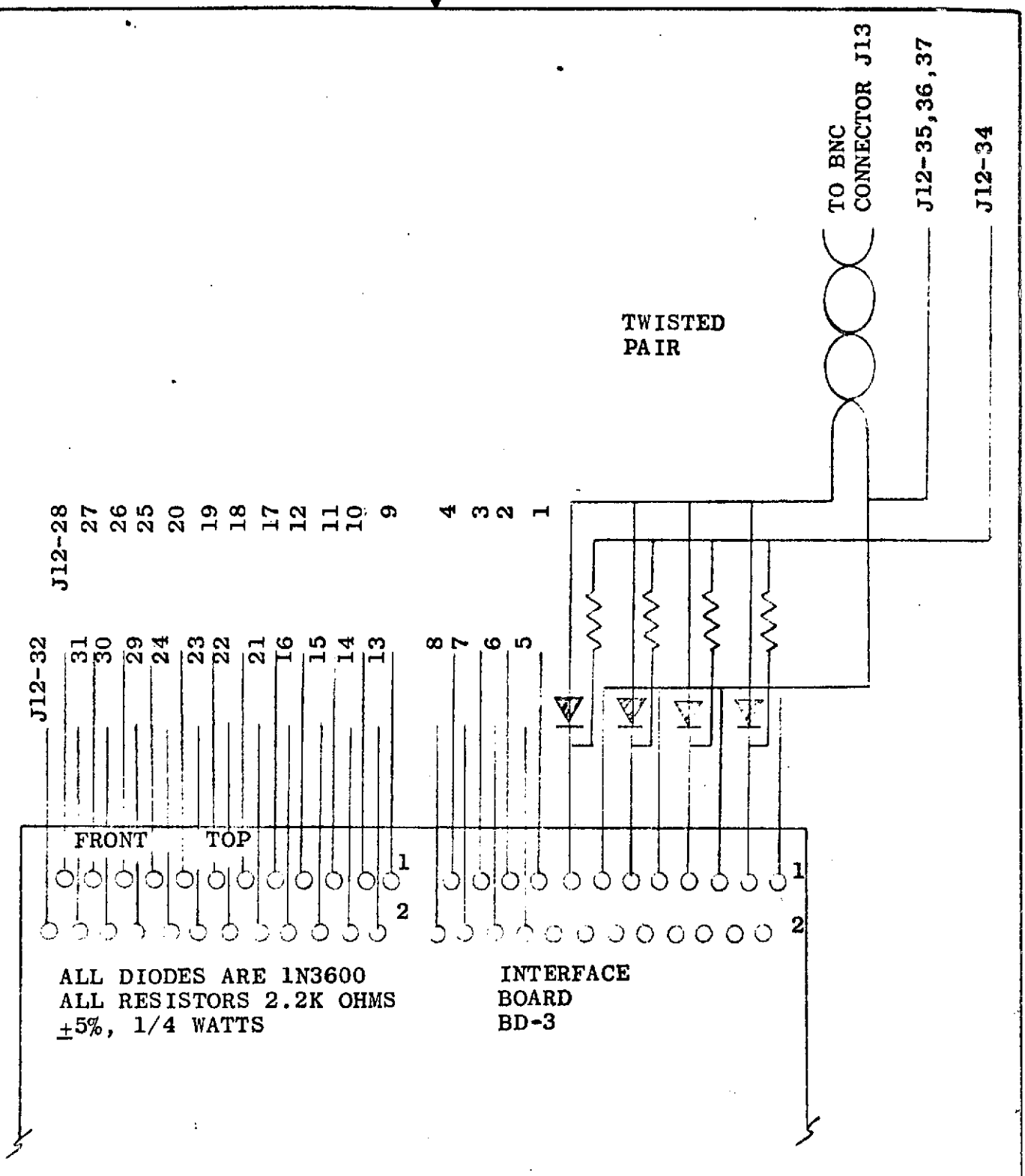

FIGURE 3: STACK TEST CABLE

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MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13729D
	SCALE	REVISION	SHEET 8

AV-2 [illegible] 100A 3/68 DWG FORMAT

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE	CODE IDENT NO.	DWG NO.	REVISION
A	94990	12-P13729D	

SCALE | SHEET 9

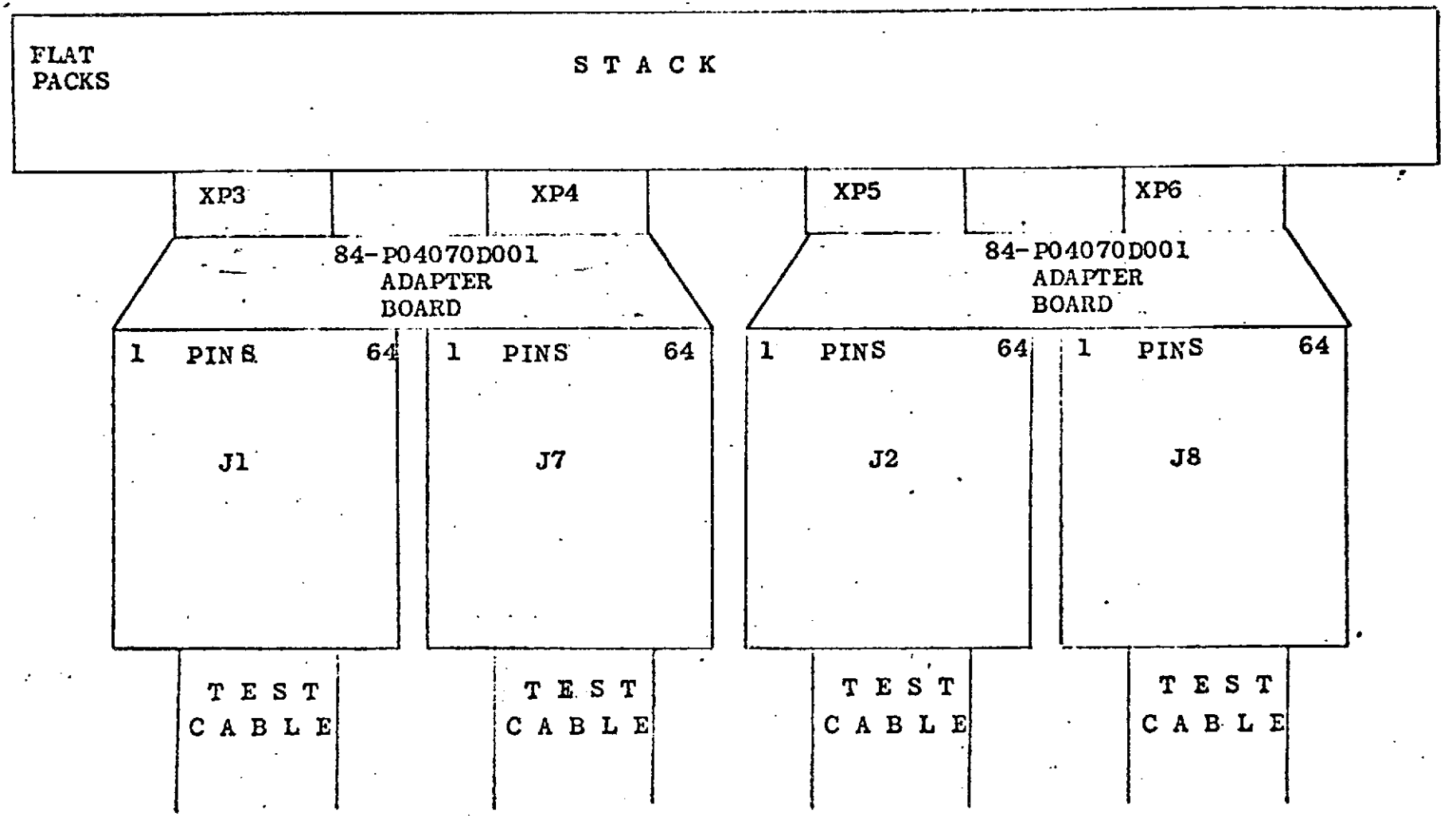

FIGURE 4

DIGIT DRIVE TEST FIXTURE INTERCONNECT

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PLATED WIRE MEMORY STACK

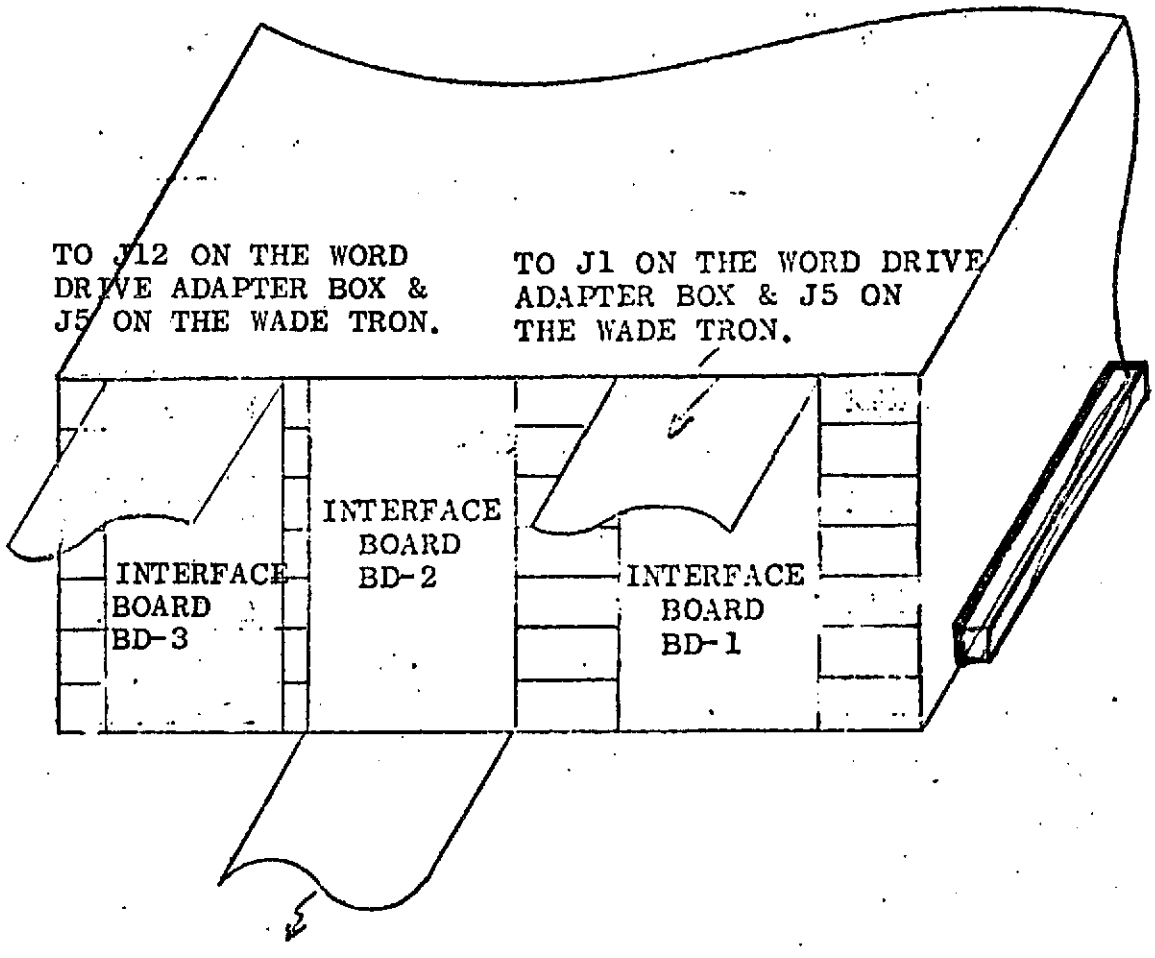

FIGURE 5 WORD LINE INTERCONNECT

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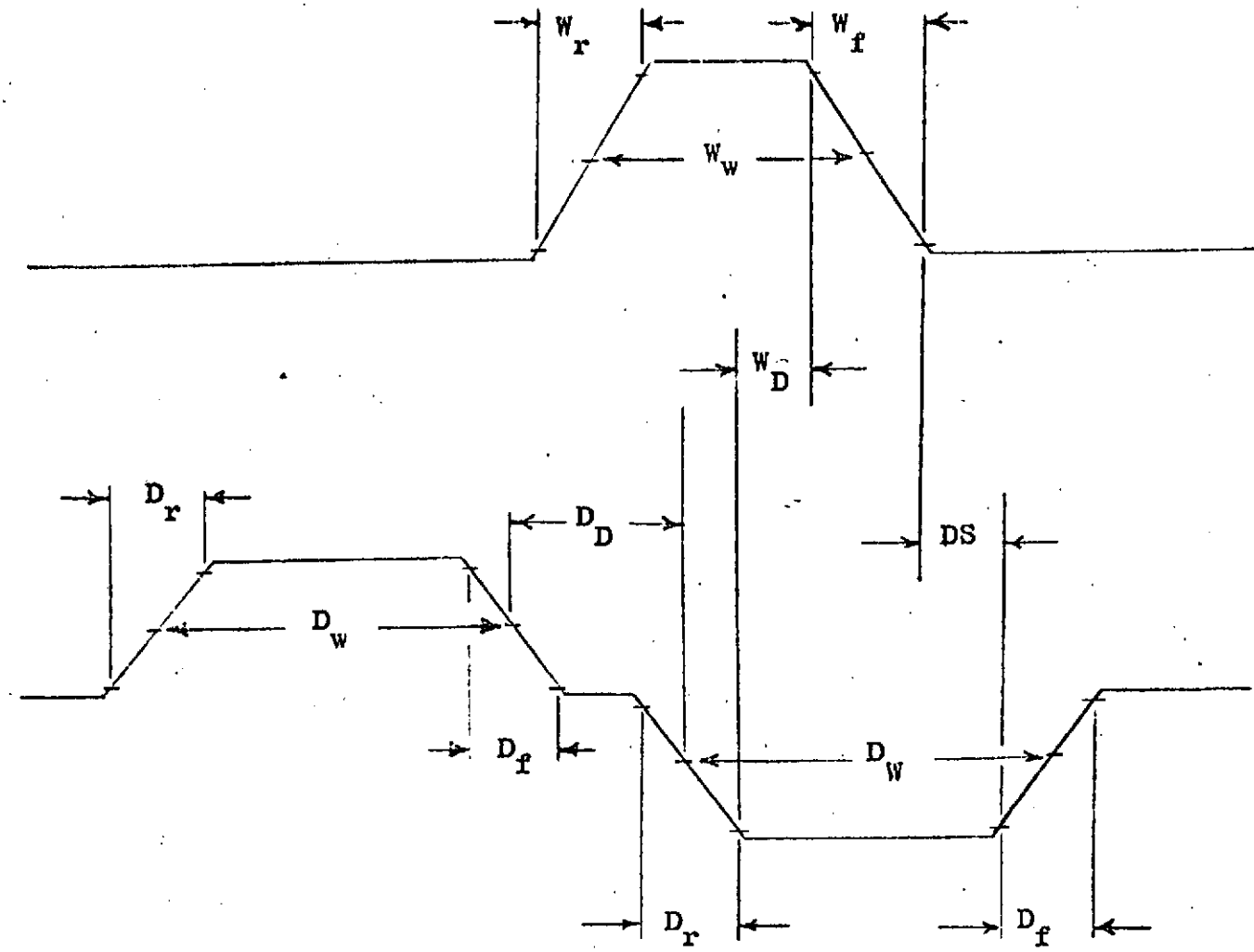
FIGURE 6 Current Waveforms



DS = 40 nanoseconds between I_W 10% & I_D 90% points.

$D_r = D_f$ = 80 nanoseconds, 10% to 90%

D_W = 220 nanoseconds, between 50% points.

D_D = 150 nanoseconds, between 50% points.

W_r = 75 $^{+5}_{-0}$ nanoseconds, 10% to 90%.

W_W = 200 ± 10 nanoseconds, between 50% points.

W_D = 60 nanoseconds, between 90% points.

W_f = 40 nanoseconds 10% to 90%

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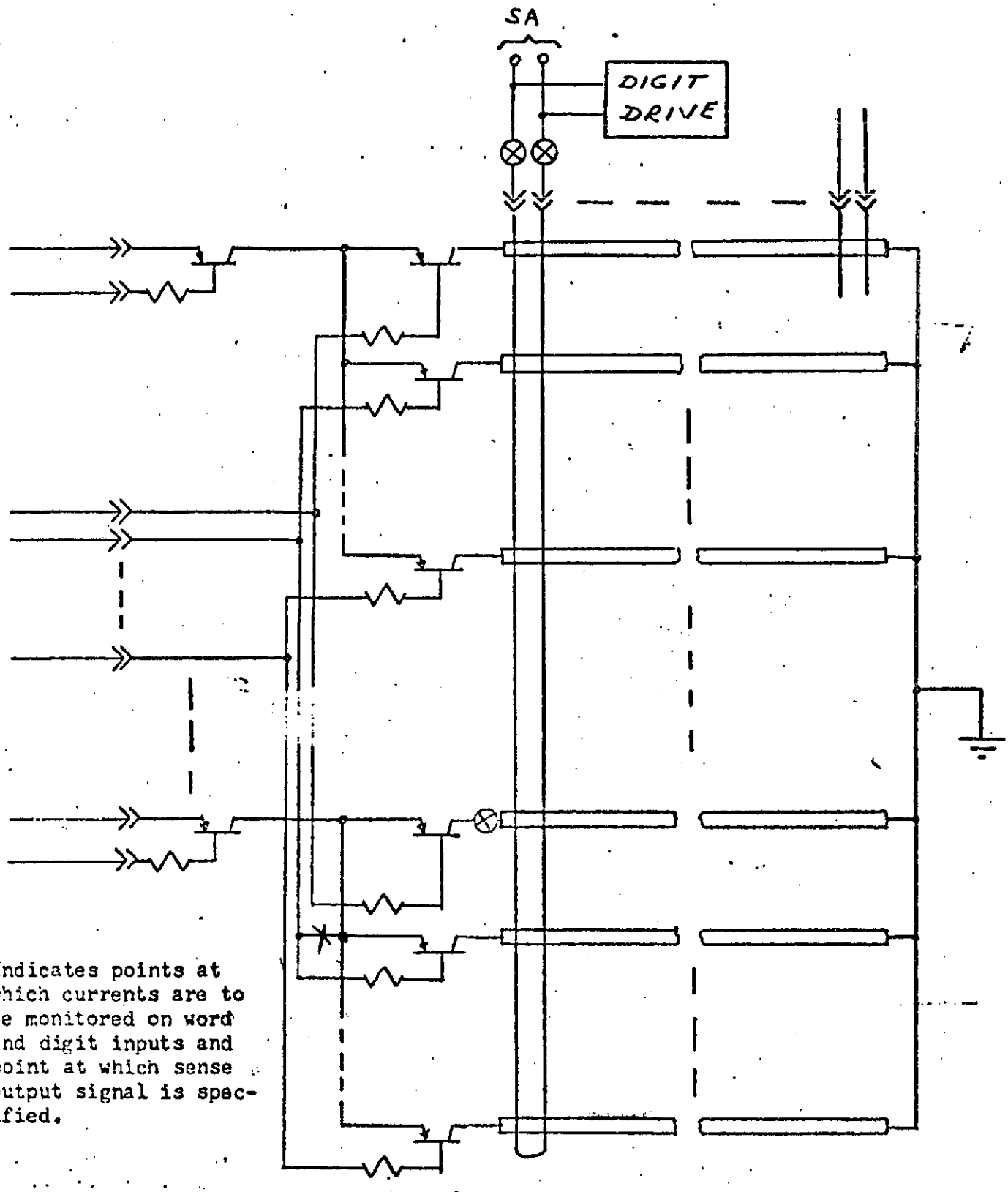
MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13729D
	SCALE	REVISION	SHEET 11



⊗ Indicates points at which currents are to be monitored on word and digit inputs and point at which sense output signal is specified.

FIGURE 7

Current Monitoring Points

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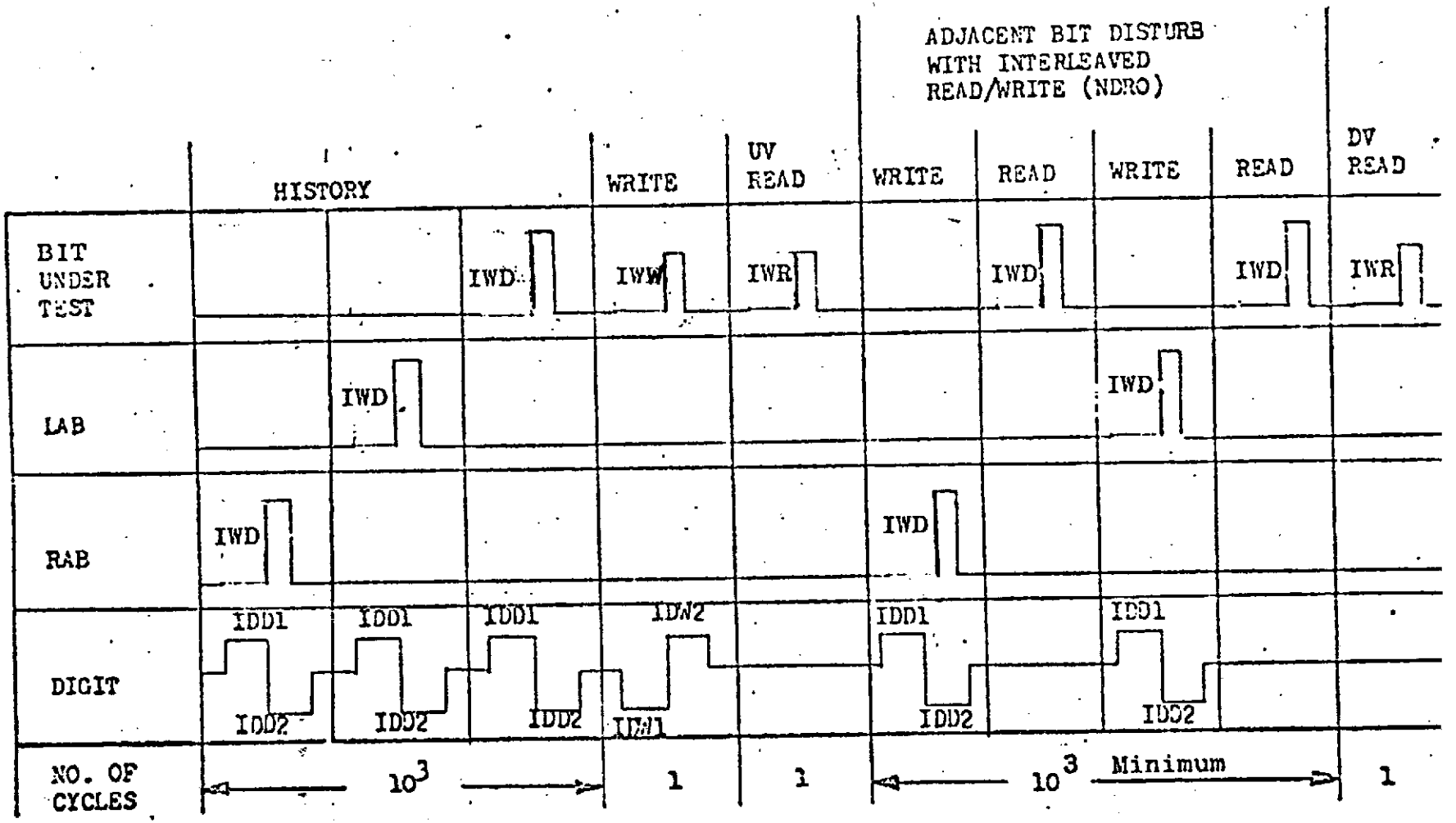


ENTIRE PROGRAM REPEATED WITH OPPOSITE POLARITY DIGIT CURRENTS

FIGURE 8: TEST PATTERN

ASTERISK INDICATES DATA WHICH IS NONMANDATORY —FOR INFORMATION ONLY.

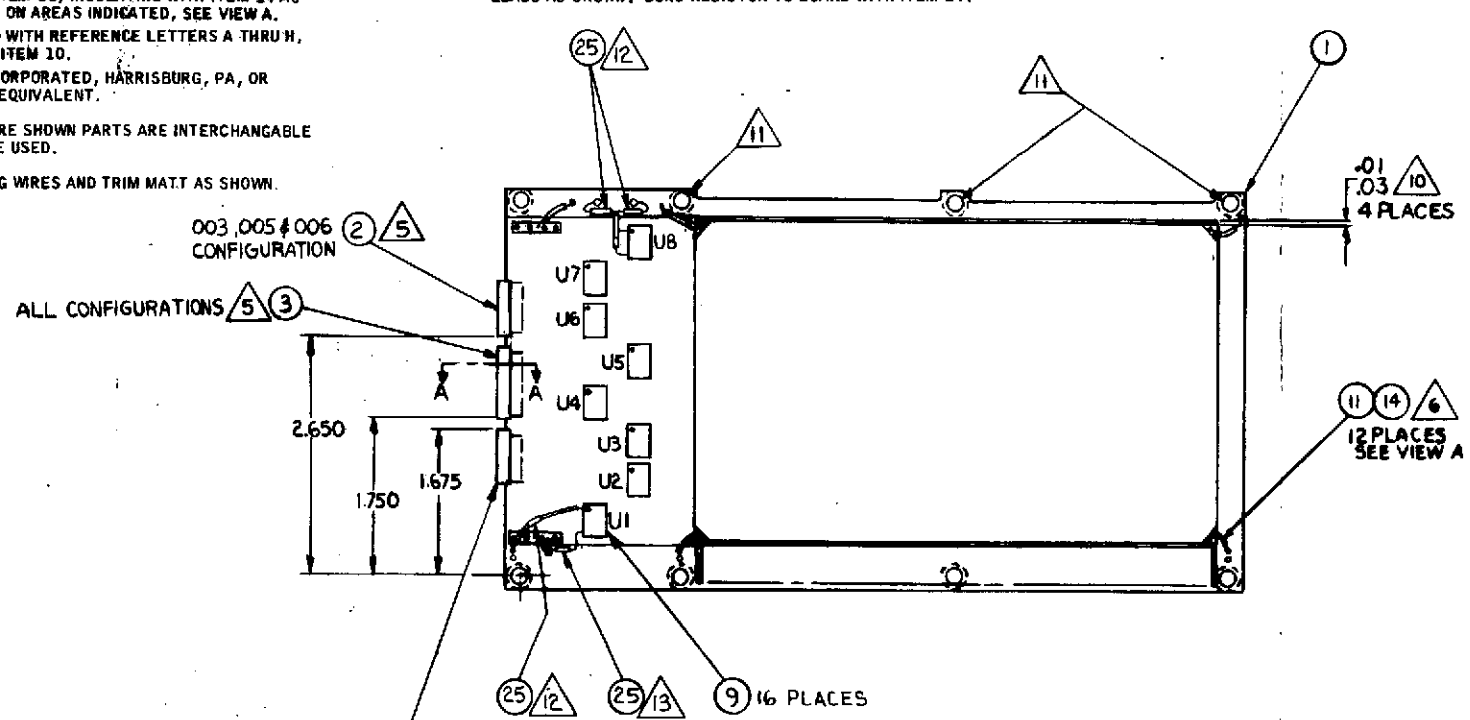
PROJECT CONTROL	LTR	DESCRIPTION	DATE	APPROVED
	—	INITIAL RELEASE		

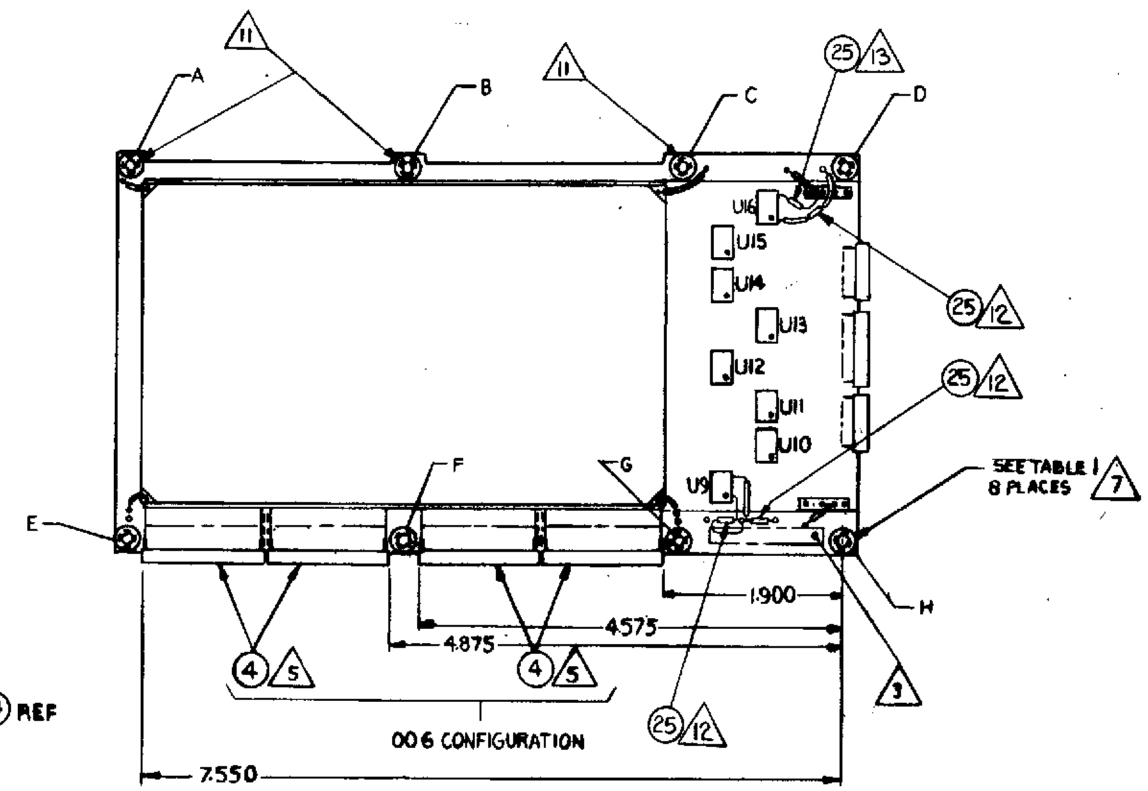
REVISIONS

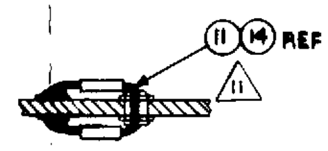
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED NOTE 6 & 7. CHANGED NO OF JUMPER WIRES FROM 16 TO 12 ADDED DIMENSION FOR MOUNTING CONNECTORS	20 FEB 73	
	B	ADDED NOTE 11 AND NOTE 11 FLAG CALLOUTS	19 JUN 73	HRT
	C	ADDED ITEMS 25 AND 26. ADDED NOTES 12 AND 13.	20 DEC 73	

NOTES:

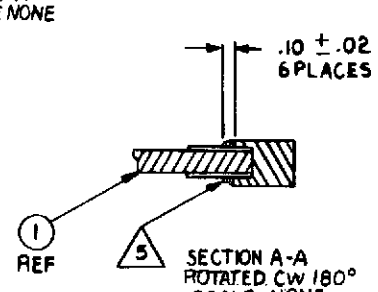
1. PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 1A1A2.
2. REFERENCE NUMBERS ARE FOR INFORMATION ONLY. THE PARTS ARE NOT MARKED.
3. △ MARK PART NUMBER AND SERIAL NUMBER APPROXIMATELY AS SHOWN IN .12 HIGH CHARACTERS OF NORMAL GOTHIC TYPE USING ITEM 12.
4. SOLDER USING ITEM 13.
5. △ LEADS ON CONNECTOR ITEM 2, 3 AND 4 SHALL BE LAP SOLDERED TO PRINTED CIRCUIT CONDUCTIVE PATTERN, AND MAY BE FIXED WITH ITEM 10. SEE SECTION A-A.
6. △ INSTALL JUMPER WIRE, ITEM 11, INSULATING WITH ITEM 14 AS INDICATED. LAP SOLDER ON AREAS INDICATED, SEE VIEW A.
7. △ INSERT ITEMS INDICATED WITH REFERENCE LETTERS A THRU H, TABLE 1 AND BOND WITH ITEM 10.
8. AS SUPPLIED BY AMP INCORPORATED, HARRISBURG, PA, OR ENGINEERING APPROVED EQUIVALENT.
9. WHERE TWO PART NO'S ARE SHOWN PARTS ARE INTERCHANGABLE AND EITHER PART MAY BE USED.
10. △ REMOVE TUNNEL FORMING WIRES AND TRIM MAT.T AS SHOWN.
11. △ INSURE THAT SPACERS, BOTH THOSE INSTALLED AND THOSE THAT WILL INTERFACE, DO NOT SHORT ON GROUND WIRE SOLDER JOINT OR PADS PROVIDED FOR GROUND WIRES ON MOTHERBOARD. IF INTERFERENCE OCCURS PADS AND SOLDER JOINT MAY BE CUT AWAY TO PROVIDE CLEARANCE. IF PART OF PAD IS CUT AWAY WHERE A KEEPER GROUNDING WIRE ITEM 11 AND 14 IS INSTALLED, THE WIRE IS TO BE REMOVED.
12. △ INSTALL RESISTOR, ITEM 25, INSULATING LEADS WITH ITEM 26 AS INDICATED. SOLDER LEAD TO PLATED THRU HOLE AND LAP SOLDER OTHER LEAD AS SHOWN. BOND RESISTOR TO BOARD WITH ITEM 14.
13. △ INSTALL RESISTOR, ITEM 25, AS INDICATED. LAP SOLDER LEADS AS SHOWN. BOND RESISTOR TO BOARD WITH ITEM 14.





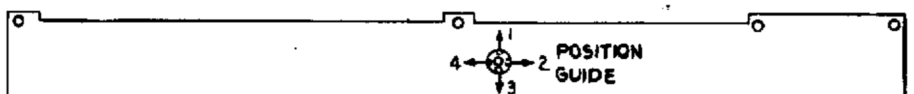


VIEW A
SCALE NONE



SECTION A-A
ROTATED CW 180°
SCALE: NONE

TABLE 1
SPACER ORIENTATION



REF DESIG	BOARD PART NO.	HOLE IDENT. AND POSITION. "A" THRU "H" INDICATES FIND NO.															
		A	POSN	B	POSN	C	POSN	D	POSN	E	POSN	F	POSN	G	POSN	H	POSN
A1 A7	001 005	7	4-1	5	—	6	1	6	2	6	4	5	–	5	–	6	2
A2, A3 A5, A6	002 003	6	4	5	—	5	–	6	2	6	4	5	–	5	–	6	2
A4	004	6	4	6	1	5	—	6	2	6	4	5	–	5	–	6	2
A8	006	8	4	8	3	8	3	8	2	8	4	8	1	8	1	8	2

SYM	SIZE	QTY

HOLE LIST

01-P13720D006	01-P13720D005	01-P13720D004	01-P13720D003	01-P13720D002	01-P13720D001	MOTOROLA PART NUMBER

NEXT ASSEMBLY	USED ON
01-P13707D	

*APPLICATION

FIND NO.	004	003	002	001	CODE IDENT NO.	DRAWING OR DOCUMENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO.	NOTE
	QTY REQD									

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR ASSOCIATED LISTS SEE PL01-P13720D

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND END USE TOLERANCES:
2 PLACE DEC ± .01 HOLE DIA + −
3 PLACE DEC ± .005

MATERIAL: △

FINISH: △

DR BY L. McNETT 5 JAN 73
CHK BY
MFG
PROJ NO. 4339
CONTRACT NO. NAS 5-23163
RELEASE NOTICE & DATE
APPROVED [signature] 1-29-73 NAME DATE
APPROVED [signature] 1-29-73 NAME DATE

MOTOROLA INC. Government Electronics Division / 8201 East McDowell Road Scottsdale, Arizona 85252

MEMORY PLANE ASSEMBLY

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SIZE D | CODE IDENT NO. 94990 | DRAWING NO. 01-P13720D

SCALE 1/1 | WEIGHT — | SHEET 1 OF 1

DWG NO. 01-P13720D

FOLDOUT FRAME

FOLDOUT FRAME